FINAL REPORT

FOR PROJECT IRLS

INTEGRATION SUPPORT

EQUIPMENT

JULY 1967

CONTRACT NO. NAS 5-10278

PREPARED BY

RADIATION SYSTEMS DIVISION
A DIVISION OF RADIATION INCORPORATED
MELBOURNE, FLORIDA

FOR

CODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

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ABSTRACT

This report describes the IRLS Integration Support Equipment designed, manufactured and tested under Contract No. NAS5-10278 for Goddard Space Flight Center, Greenbelt, Maryland. It also provides a comprehensive discussion on the overall characteristics of the Interrogation, Recording, and Location Subsystem and the conclusions and recommendations derived from this project, The requirements of this contract were satisfied with complete adherence to GSFC Specification, IRLS Integration Support Equipment, S-731-P-20 dated 7 January 1966. This specification is contained in Appendix I of this report. Minor deviations from the proposed configuration were incorporated into the final end item. These changes were in the interest of conservation of components, logic simplification, and increased testing flexibility. The only significant change from the proposed operational sequence was the utilization of the platform modulator driver in the power control and distribution module as the signal driving mechanism for the self-check tester output. This change enhanced operational verification of the modulator driver circuits and reduced the number of components.

All test data that indicates adherence to the specification is included and shipped with each data package supplied with individual units. No requirement for environmental testing was invoked by the specification due to equipment utilization in a laboratory environment. Printed-circuit card temperature tests were performed on the power supply card as a design proof test by using a temperature range of -10°C to +50°C and a voltage range of -24.5±2 vdc. All other components were specified for a temperature range of 0°C to +50°C with greater than 10 percent voltage variations.

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SECTION I

INTRODUCTION

1-0. INTRODUCTION.

1-1. SCOPE AND PURPOSE.

This document provides a detailed report of the effort accomplished by Radiation Incorporated for the NASA Goddard Space Flight Center under jurisdiction of Contract No. NAS 5-10278 pertaining to the Integration Support Equipment (ISE) used in the Interrogation, Recording, and Location Subsystem (IRLS). Radiation Incorporated was awarded this contract to design, develop, and test three units of Integration Support Equipment for use during the IRLS Nimbus B Experiment.

1-2. CONTENT.

Section I of this report introduces the primary tasks specified under Contract No. NAS 5-10278 and also provides a complete introduction to the operational sequences, functions, and major characteristics of the overall IRL Subsystem. Section II describes the function of the ISE and defines the physical and electrical characteristics of the overall configuration and individual drawer assemblies within the rack. Applicable documents that are referenced throughout this report are also contained in this section. The third section provides a functional block diagram description of the Integration Support Equipment as the unit operates in its various modes. A chronological history comprised of problem areas, solutions, and completion dates is provided in Section IV. Section V contains the conclusions and recommendations derived from this project.

1-3. IRL SUBSYSTEM INTRODUCTION.

1-4. General

It is necessary to the understanding of the function of the Integration Support Equipment that a functional description of the overall operation of the IRL Subsystem be included in this report. IRLS equipment is used in conjunction with the Nimbus spacecraft and provides for accurate and efficient collection of various types of data from areas remote to normal traffic flow on a global scale. Requirements for such data gathering equipment in the meteorological and oceangraphic fields have been a foremost consideration in the synthesis of the IRLS concept. As a result, design of the IRLS equipment provides the capability of determining the range and tracking the location of mobile unmanned data stations (platforms) in addition to the basic data gathering function.

The basic equipment components of the operational IRLS include platform unmanned data gathering stations (either mobile vehicles, such as free buoys or balloons, or fixed locations, such as remote weather stations), the IRLS satellite equipment aboard the Nimbus spacecraft, and a Ground Acquisition and Command Station (GA&CS). The unmanned data gathering stations accept analog data from transducer sensing devices and provide the circuits necessary to multiplex, encode, and transmit this information upon reception of an interrogation command from the Satellite Electronics and Telemetry Equipment. The Satellite Electronics and Telemetry Equipment provides storage of commands from the GA&CS, logic circuits necessary to process location data, the communication link with each interrogated plat-

form, storage of locationand platform sensor data, and the communication link with the GA&CS. The GA&CS functions as the centralized data collection and processing installation and command generation post for the IRL Subsystem.

A simplified functional block diagram of the overall IRL Subsystem is shown in Figure 1. Platform interrogation command data is introduced into the IRL Subsystem via a punched tape program that is inserted into the memory system of the GA&CS. The command data is read out of the GA&CS memory system and transmitted when the orbiting IRLS satellite enters communication view of the GA&CS during an orbital pass around the earth, This interrogation command data information is stored in the IRLS satellite command memory and programs the IRLS satellite to communicate with selected platforms during the subsequent orbits. At preprogrammed time intervals, when the IRL Subsystem interrogation command time and IRLS elapsed time clock coincide, the IRLS satellite begins transmission of a platform address signal. The platform selected for interrogation receives the signal, recognizes its address, and verifies its identity to the IRLS satellite. Upon platform verification, the IRLS satellite interrogates the platform, performs a ranging function that measures the satellite-to-platform distance and receives and stores the encoded data telemetered from the platform. The satellite-to-platform sequence is repeated for selected platforms until the IRLS satellite exhausts its preprogrammed communication sequence. At this time, the GA&CS forwards the appropriate command to order the IRLS satellite to transmit the information stored in the IRLS satellite data memory to the GA&CS. The GA&CS accepts and stores the encoded information in its memory system. The stored data is then punched on paper tape to be furfher processed. Also at this time, the GA&CS transmits new interrogation command data for IRLS satellite use during the next orbit or orbits.

1-5. Functional Data Flow.

1-6. General.

Information and data flow during the interrogation command and data transfer sequence between the IRLS satellite and the GA&CS is shown in Figure 2. Figure 3 depicts data flow during the platform interrogation and data transfer sequence between the IRLS satellite and platform.

1-7. GA&CS-To-Satellite Sequence.

Duringan orbit, the IRLS satellite is capable of interrogating as many as 20 platforms. The command sequence of platform interrogations is programmed at the GA&CS site for each orbit or sequence of orbits. Up to twenty 32-bit interrogation command words are inserted into the GA&CS digital data processor via a punched paper tape. This tape includes the interrogation command time for individual platforms, the correct address for each platform, and a computer analysis of spacecraft estimated time of arrival (S/C ETA). The stored interrogation program inserted by the punched tape can be initiated manually by an operator before S/C ETA or automatically whenever coincidence occurs between S/C ETA and real time. When initiated, the stored program is referenced to a 36-bit NASA time code input that represents time-of-day. A correlation occurs between the reference time-of-day and earliest command start time (ECST) input from the punched tape. A time coincidence must occur before operation of the delta time counter can be initiated. When ECST and time-of-day correlation occurs, the delta time counter counts the time difference between S/C ETA and ECST and subtracts the difference from the 15 most significant bits in the 16-bit time code portion of an interrogation command word prior to transmission of this word to the IRLS satellite. At delta time counter enable, a remote status indicator in

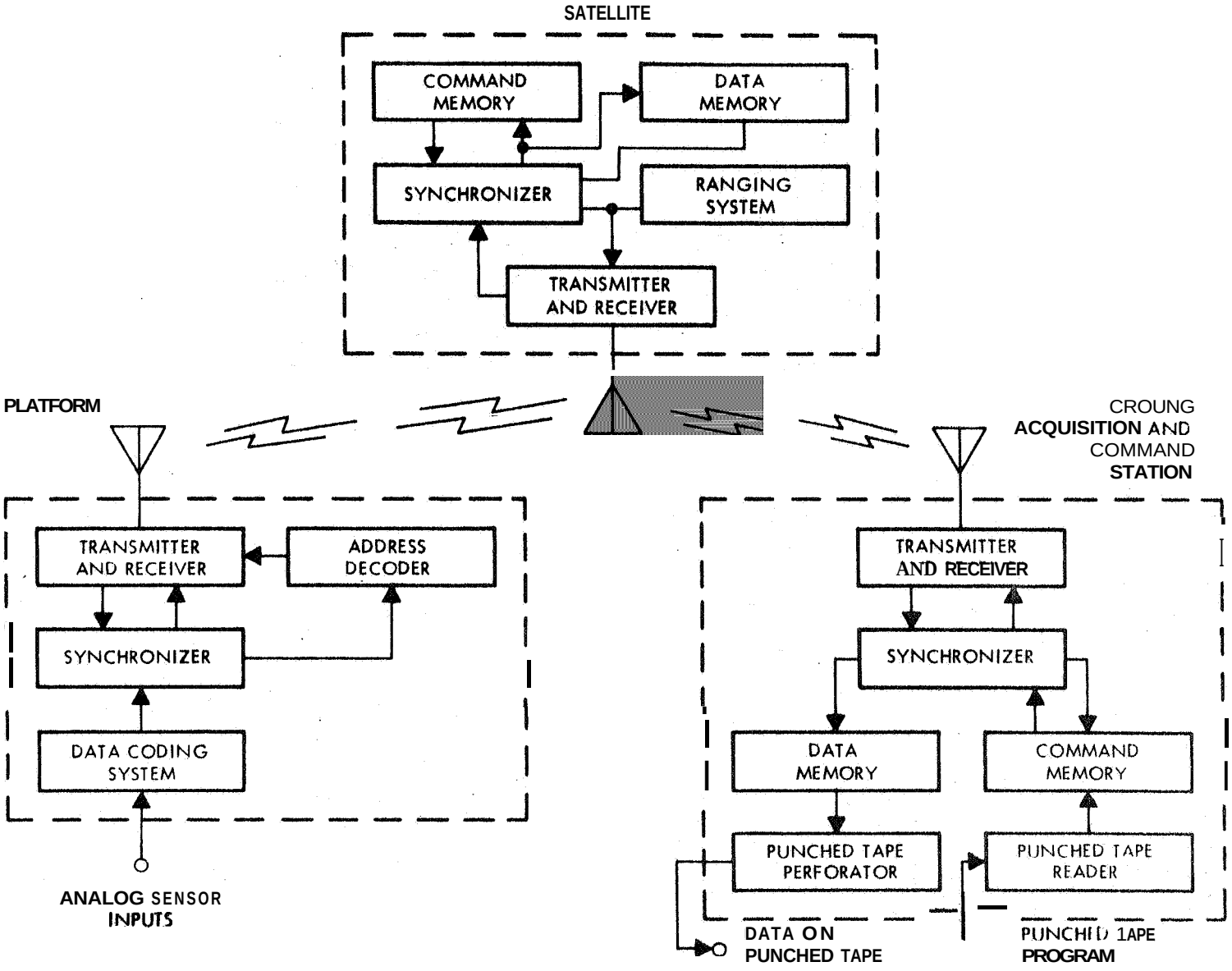
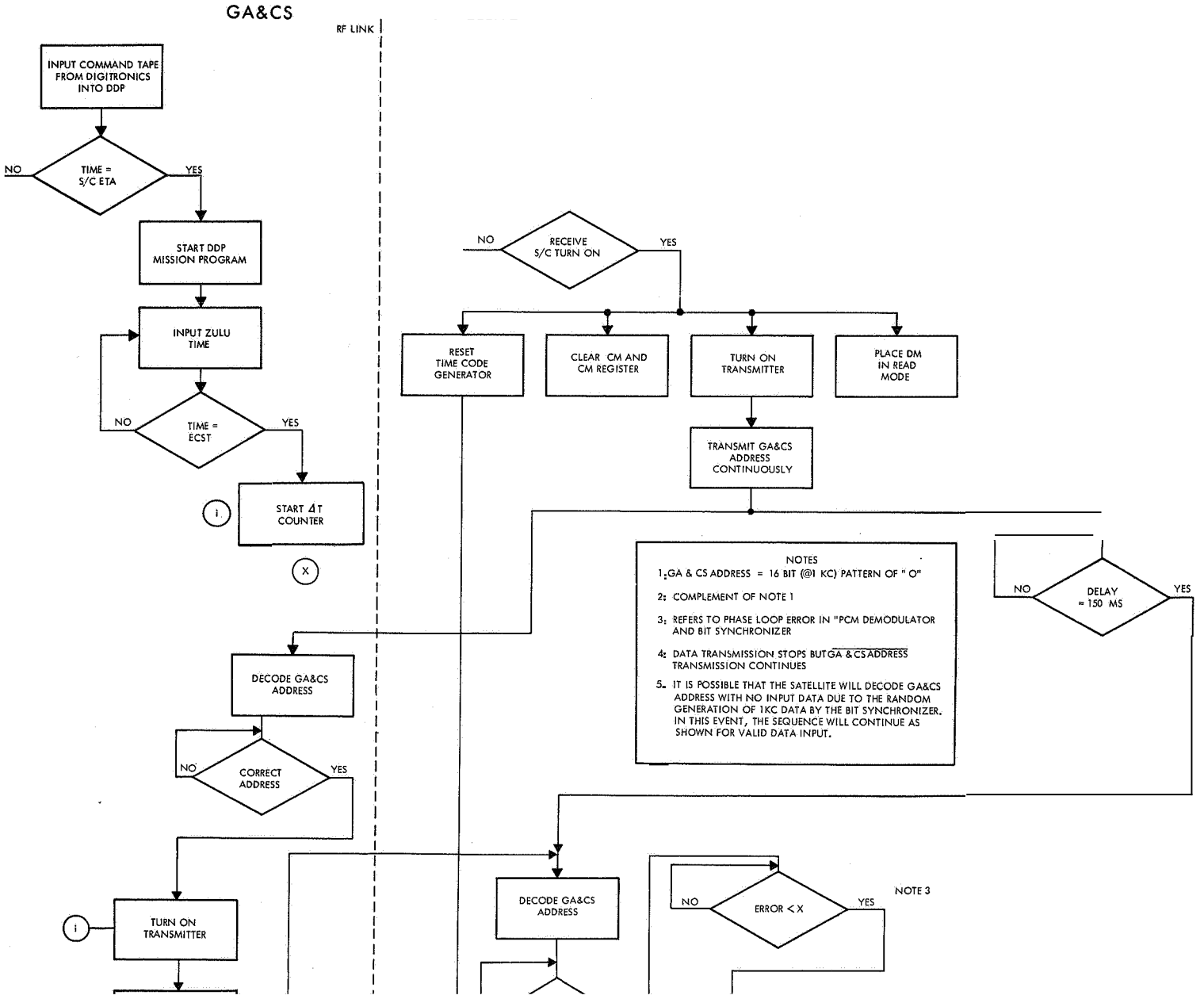


Figure1. IRLS Simplified Block Diagram.


GA&CS
RF LINK
INPUT COMMAND TAPE FROM DIGITRONICS INTO DDP
TIME = S/C ETA
NO
YES
START DDP MISSION PROGRAM
INPUT ZULU TIME
TIME = ECST
NO
YES
START ΔT COUNTER
i
X
RECEIVE S/C TURN ON
NO
YES
RESET TIME CODE GENERATOR
CLEAR CM AND CM REGISTER
TURN ON TRANSMITTER
PLACE DM IN READ MODE
TRANSMIT GA&CS ADDRESS CONTINUOUSLY
NOTES
1. GA & CS ADDRESS = 16 BIT (@1 KC) PATTERN OF " O"
2. COMPLEMENT OF NOTE 1
3. REFERS TO PHASE LOOP ERROR IN "PCM DEMODULATOR AND BIT SYNCHRONIZER
4. DATA TRANSMISSION STOPS BUT GA & CS ADDRESS TRANSMISSION CONTINUES
5. IT IS POSSIBLE THAT THE SATELLITE WILL DECODE GA&CS ADDRESS WITH NO INPUT DATA DUE TO THE RANDOM GENERATION OF 1KC DATA BY THE BIT SYNCHRONIZER. IN THIS EVENT, THE SEQUENCE WILL CONTINUE AS SHOWN FOR VALID DATA INPUT.
NO
DELAY = 150 MS
YES
DECODE GA&CS ADDRESS
NO
CORRECT ADDRESS
YES
i
TURN ON TRANSMITTER
DECODE GA&CS ADDRESS
NO
ERROR < X
YES
NOTE 3

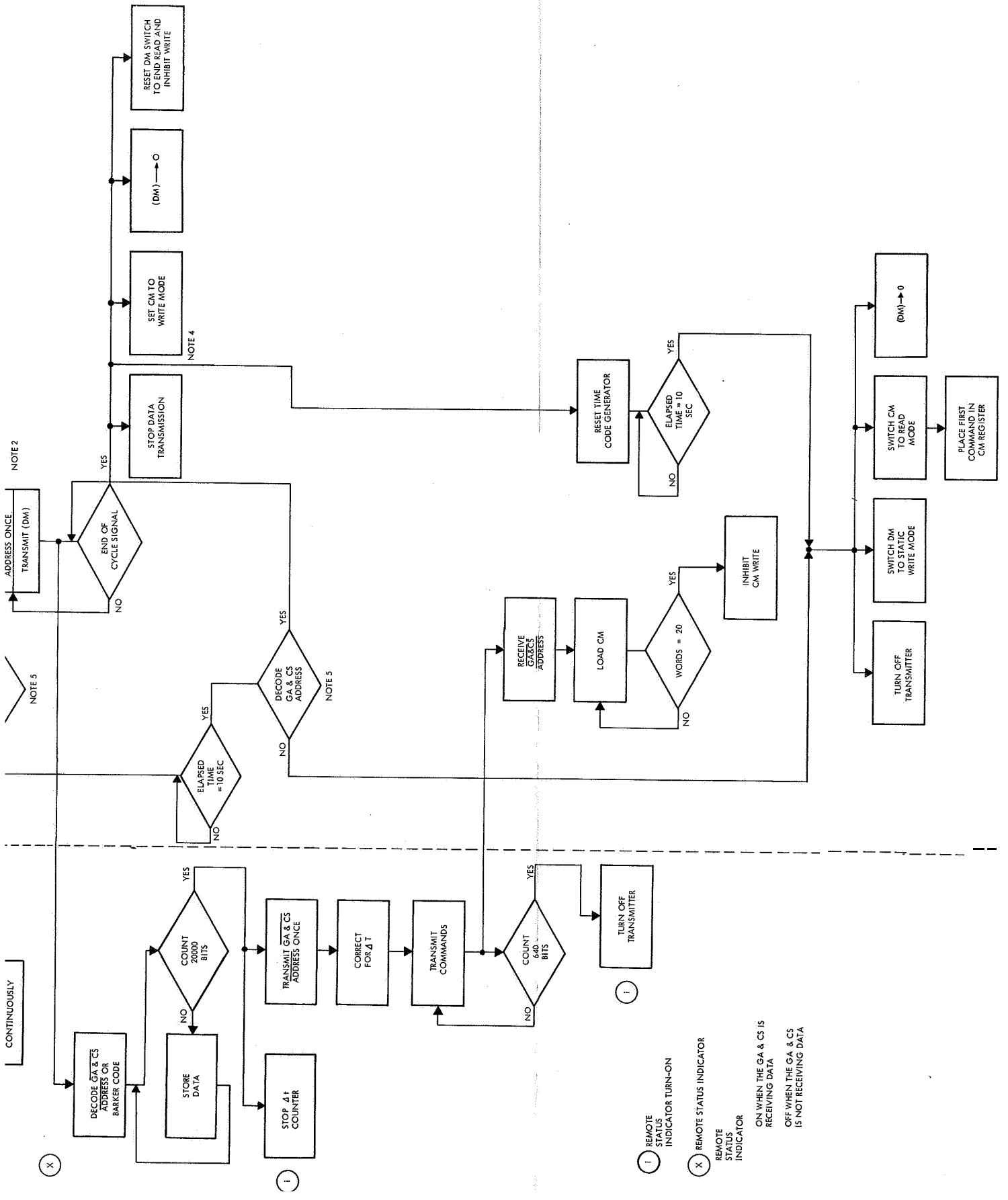


Figure 2. Satellite-to-GA&CS Flow Diagram.

the Nimbus Command and Data Acquisition (CDA) Station is energized to indicate counter operation. Also at this time, the receiver in the digital data processor begins searching for the GA&CS address as transmitted by the IRLS satellite.

Satellite transmission of the GA&CS address code is initiated by a command from the Nimbus CDA station. This command places the IRLS satellite in an operational mode by preparing it for readout of all stored data. Reception of the turn on command from the Nimbus CDA allows the IRLS satellite to clear and update the information content of the command memory and storage register, enable the data memory to read out all data stored during the previous orbit or orbits, reset the satellite time code generator to establish a timing sequence to automatically deenergize the transmitter after a specified period, and energize the transmitter to continuously transmit the stored GA&CS address code. As the GA&CS address code is transmitted, a 150 millisecond delay is initiated that inhibits decoding of the return address transmission from the ground station for that period of time.

As previously stated, the GA&CS searches for the IRLS satellite transmission of its code after initial operation of the delta time counter. After reception of the 16-bit GA&CS address code, the GA&CS compares the input address code with a code stored in the memory system, and energizes a remote status indicator in the CDA that indicates reception of address code data. If theaddress code is correct, a correlation occurs and energizes the GA&CS transmitter to transmit the GA&CS address code back to the IRLS satellite in a continuous serial pulse train. A remote status indicator in the CDA is also energized to indicate transmitter turn-on. If no correlation occurs, all GA&CS operation is inhibited except address decoding and recognition. The GA&CS address code is retransmitted to the IRLS satellite where another correlation is performed to recognize the code. During address code verification, a phase comparison between the received signal and the regenerated range word sequence within the IRLS satellite is also being performed. Performance of this signal comparison achieves phase synchronization and allows the IRLS satellite to initiate data readout. If phase synchronization cannot be obtained, data transfer from the IRLS satellite is automatically inhibited. After phase synchronization between the two signals is achieved, the IRLS satellite transmits one 16-bit pattern of the GA&CS address complement code $\overline{\text{(address)}}$ and then begins readout of all encoded datastored in the memory during the previous orbit or orbits. Upon reception of the data, a remote status indicator is energized in the CDA for a visual indication of data reception.

The GA&CS must receive, decode, and recognize the IRLS satellite transmission of the GA&CS address code or a barker word before allowing the memory to count and store up to 20,000 major bits of encoded information that originated in the IRLS platforms. Loading of the GA&CS memory is automatically inhibited after storage of the last data bit. After the satellite data memory has completed readout, an end-of-cycle signal is derived that inhibits data transmission but allows GA&CS address code transmission to continue, enables the satellite command memory to receive new interrogation command words, ensures that all positions in the data memory contains ONE's and is not capable of entering data, and initiates a secondary timing sequence to ensure proper event programming.

Storage of the last data bit in the GA&CS memory inhibits operation of the delta time counter, energizes a remote status indicator, and allows transmission of one 16-bit pattern of the GA&CS address code. Correction between the delta time value and the punched tape

interrogation command time program is accomplished before transmission of new 32-bit interrogation command words to the IRLS satellite. Transmission of the 32-bit interrogation command words is inhibited after the GA&CS verifies that 640 bits of information have been transmitted. The GA&CS transmitter is deenergized at this time.

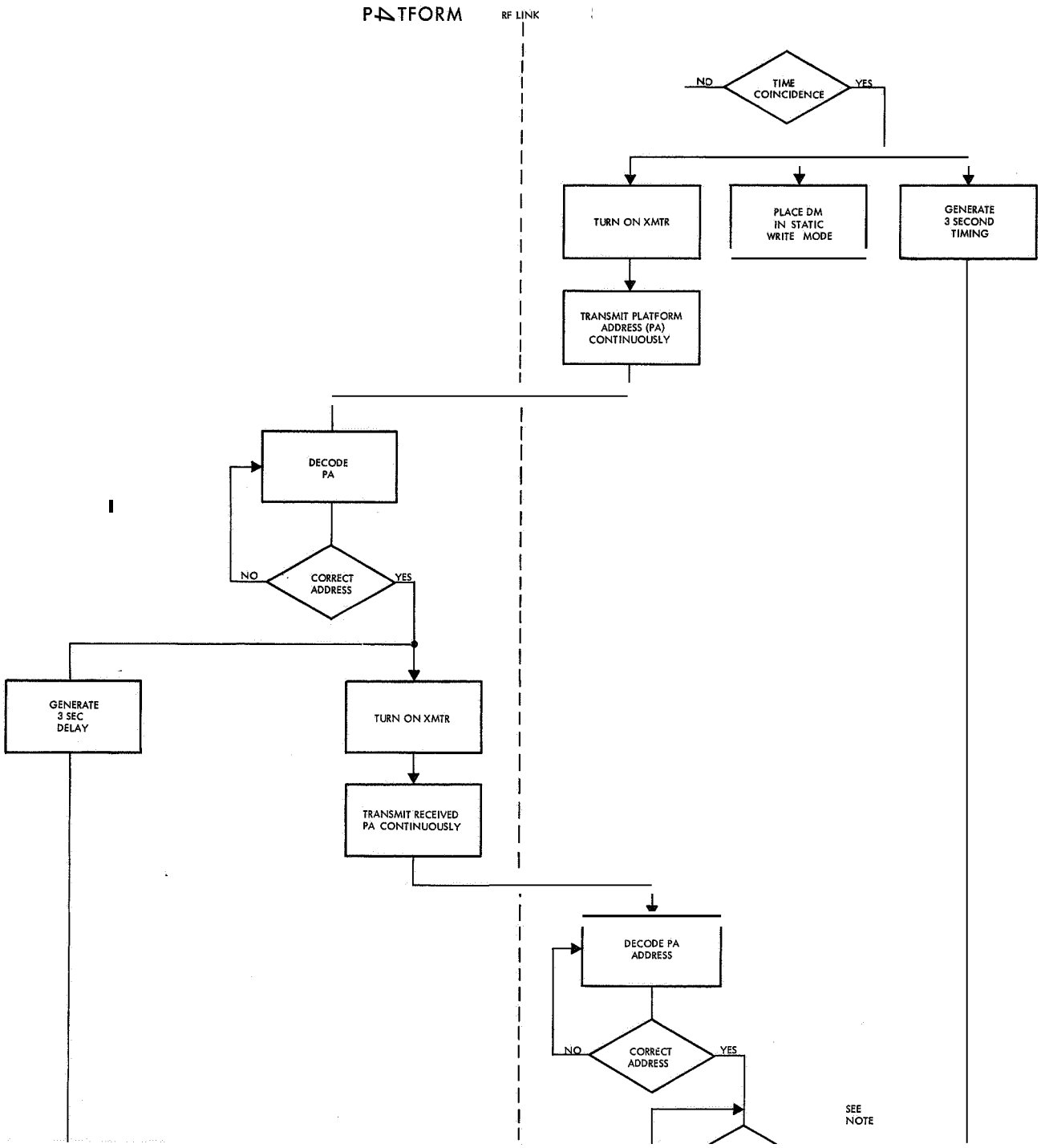
The IRLS satellite receives the GA&CS address code bit pattern and up to 20 interrogation command words and loads this information into its command memory. The memory loading process continues until the 20 interrogation command words are written in the command memory.

Resetting the IRLS satellite time code generator upon reception of the turn-on command from the CDA enables a ten-second elapsed time counter. At the end of 10-seconds, the counter enables a sampling of the GA&CS address code verification process. If the GA&CS address has not been decoded and verified at the end of ten seconds, a turn off command is automatically supplied to the transmitter, the read mode of the data memory is inhibited, andthedata memory is cleared and placed in a static mode of operation. If the 10-second sampling determines that the GA&CS address code has been verified, operation continues until the end-of-cycle signal is generated at the end of 21 seconds. At this time, the 10 second elapsed time counter in the time code generator is reset for another 10-seconds. At the termination of this 10-second period, the transmitter is turned off, the data memory is inhibited and all locations are reset to ONE's,and a new interrogation command word is placed in the command memory storage register.

1-8. Satellite-to-Platform Sequence.

During an IRLS satellite orbit, a 32-bit interrogation command word from the satellite memory is shifted into a storage register where it is divided into 16-bits that represent the selected platform address code and 16-bits that determine the time of interrogation. The 15-MSB bits representing interrogation time is continuously compared to the IRLS time reference until time coincidence occurs. When an interrogation time correlation is achieved, the IRLS satellite prepares the data memory to receive information from the platform, enables a 3-second counter, and provides a turn-on command to the transmitter. Transmitter turn on enables the IRLS satellite to continuously transmit the 16-bit platform address code until recognition and response from the platform or until the 3-second counter reaches an elapsed time of 3.0 seconds.

The platform receives the continuously transmitted address code and determines code validity by comparing it with a preassigned code that is hardwired into the unit. If the received address code is incorrect, the platform inhibits all operation except address code recognition until address code correlation is achieved, When the address code *is* recognized, the platform enables a 3-second counter and energizes its transmitter to enable continuous transmission of the received platform address back to the IRLS satellite. Upon reception of the retransmitted platform address code, the IRLS satellite verifies that the input code matches the 16-bit address code from the command memory. If not, all IRLS satellite operation, except address code transmission and correlation, is inhibited until coincidence occurs. A phase synchronization comparison between the received platform address code and the regenerated range word sequence is also perforrned at this time. If the phase lock error is too great and phase synchronization has not been achieved, IRLS satellite decoding of the platform


PLATFORM
RF LINK
NO
TIME COINCIDENCE
YES
TURN ON XMTR
PLACE DM IN STATIC WRITE MODE
GENERATE 3 SECOND TIMING
TRANSMIT PLATFORM ADDRESS (PA) CONTINUOUSLY
DECODE PA
NO
CORRECT ADDRESS
YES
GENERATE 3 SEC DELAY
TURN ON XMTR
TRANSMIT RECEIVED PA CONTINUOUSLY
DECODE PA ADDRESS
NO
CORRECT ADDRESS
YES
SEE NOTE

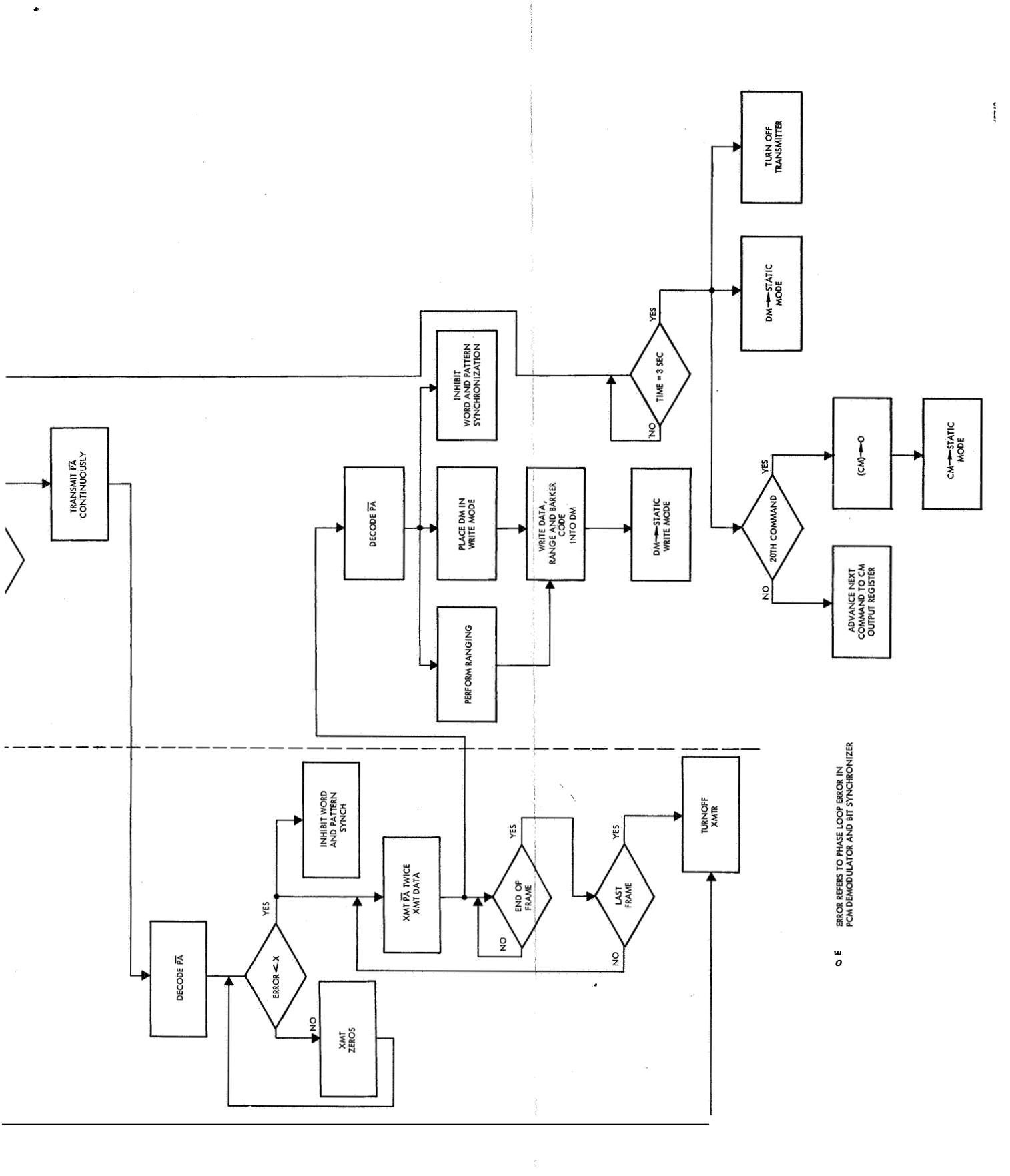


Figure 3. Platform–to–Satellite **Flow** Diagram.

address is inhibited until phase lock between the two signals is obtained. If the phase lock error is within tolerance, the IRLS satellite switches its UHF transmission to the platform address code complement ($\overline{\text{address}}$) and provides continuous transmission of this code to the platform.

The platform accepts and recognizes the $\overline{\text{address}}$ code transmission while, at the same time, a phase comparison between the received signal and the regenerated range word sequence within the platform is being performed. Performance of this signal comparison achieves phase synchronization and enables initiation of data generation within the platform. After address code recognition and phase lock, the platform inhibits generation of word and pattern synchronization signals and begins transmission to the IRLS satellite. Before actual data generation and transmission, the platform transmits two platform address codes to the IRLS satellite to condition the data memory for reception of encoded data. The IRLS satellite decodes the received platform address code and inhibits generation of word and pattern synchronization signals, enables the data memory to record and store encoded data, and performs a ranging function to establish the position of the platform.

A platform may encode and transmit one through six data frames containing 28 through 168 data words (7-bits each) of information, respectively. This information, in conjunction with ranging and barker code information, is written and stored in the IRLS satellite data memory for subsequent readout to the GA&CS. After transmission of two platform address codes, 28 data words, and a third platform address code, the platform generates a signal indicating end-of-frame. If only one data frame is transmitted, this end-of-frame signal initiates generation of a signal signifying the last frame, which, in turn, produces a turn-off command to the platform transmitter in order to terminate platform-to-satellite communication. If more than one data frame is to be transmitted, the signal identifying the last frame is not generated and the data frame sequence, initiated by transmission of two platform address codes, is forwarded to the IRLS satellite. If data frame transmission is not completed within an elapsed time of 3.0 seconds, the 3-second counter in the platform automatically terminates communication between the two units.

At the end of three seconds, the IRLS satellite data memory is placed in a static mode, the command memory prepares the IRLS satellite for the following interrogation cycle, and a turn-off command to the transmitter is generated. When all interrogation sequences have been performed and all command information has been read out the command memory, all ZERO's are loaded into the storage register.

1-9. Functional Operations.

1-10. General.

The equipment within the IRL Subsystem performs the three basic functions of interrogating an unmanned data gathering platform, recording the encoded data in the IRLS satellite and the GA&CS, and locating the position of the platform by performance of a ranging function in the IRLS satellite. The following paragraphs provide a description of the three functions performed by the IRL Subsystem.

1-11. Interrogation

The interrogation function allows the IRLS satellite aboard the Nimbus spacecraft to communicate with any selected platform, The platform interrogation sequence is programmed for a single or successive orbits at the GA&CS site. Each platform is assigned a discrete address code consisting of a digitally coded number containing 16 bits. An interrogation command, as stored in the satellite command memory, consists of two parts:

a. The address code of the platform to be interrogated; and

b. The exact time, referenced to IRLS satellite orbit time, that the platform is to be interrogated.

These two requirements are met by assigning a command word to each interrogation. Each GA&CS command word is digitally coded and consists of 32-bits, 16 specify a particular address and the fifteen most significant bits in the second 16-bit sequence specify time of interrogation command transmission. A stable clock aboard the Nimbus spacecraft is used to control the time of execution of critical operations throughout any one orbit. This same clock is used in the IRLS to synchronize a counter in order to develop a 16-bit code word corresponding to the orbit time relative to zero and is updated each 0.4 second of real time. The coding arrangement is simple binary coding and corresponds to the coding arrangement of each interrogation command word. Thus, a means of developing a time code in the satellite that can be compared to any time code in an interrogation command word is achieved.

Once a platform interrogation sequence is programmed by a computer external to the GA&CS, a selected series of 32-bit interrogation command words is generated and punched onto paper tape. The total number of interrogation commands necessary is dependent upon the deployment of the remotely located platforms relative to the subsequent satellite orbit around the earth. When the IRLS satellite is in communication view of the GA&CS located at Fairbanks, Alaska or Rosman, North Carolina, a command from the GA&CS is routed via the Nimbus spacecraft command system to the IRLS satellite. This command performs two functions:

a. The IRLS clock is reset to zero time in the counter; and

b. The IRLS communication system between the IRLS satellite and GA&CS is turned on, allowing the GA&CS to receive stored information from the satellite data memory that was processed during the previous orbit or orbits and to load a new sequence of interrogation command words into the satellite command memory.

On the Nimbus spacecraft, the IRLS satellite contains a command memory that enables it to store all Interrogation command words transmitted by the GA&CS in order to control the platform interrogation sequence. This command memory is comprised of magnetic cores and is large enough to accommodate 20 interrogation command words of 32-bits each. When all command signals from the GA&CS are received and stored in the satellite command

memory, communication between the two is terminated and the IRLS satellite aboard the Nimbus spacecraft initiates its platform interrogation sequence. During this sequence, the first interrogation command word received in the satellite command memory is read into a storage register where it is divided into two distinct parts, 16-bits specifying platform address code and 15-MSB bits that determine the time of interrogation. The 15-bit time code portion is continuously compared to the IRLS elapsed time counter until the occurrence of a correlation between the two. At this time, the IRLS satellite is instructed to interrogate the first platform. Interrogation is accomplished by serially transmitting the address code of that particular platform at the rate of 1041 bits per second as a digital modulation superimposed on the fundamental IRLS bit rate of 12.5-kilobits/second digital subcarrier. Transmission of the 16-bit address code continues until the platform responds or the total time for a complete interrogation sequence for any platform exceeds 3.0 seconds. If no response, the command word for the next platform interrogation sequence is placed in the IRLS satellite command-memory storage register.

Each platform contains an address correlator that compares any incoming 16-bit address code with a preassigned address code that is hardwired in the platform before positioning in a remote location. When the address correlator determines that the received address code matches the assigned address code, the platform energizes its UHF transmitter and replies on the IRLS frequency channel by transmitting its own address back to the IRLS satellite.

The IRLS satellite receives the platform transmission and determines the validity of the signal through utilization of an address verification detector. If the platform address is verified, the IRLS satellite switches its UHF transmission to the complement of the platform address and relays this to the platform and also prepares the data memory to receive and store encoded data from the platform.

The platform must recognize the address code complement transmission from the IRLS satellite before initiating transmission of encoded data. When recognition is achieved, data is transmitted from the platform to the IRLS satellite data memory for storage. On completion of an interrogation sequence, the satellite data memory stores all encoded data until the Nimbus spacecraft receives a data readout command from the CDA. At this time, the stored data is transmitted to the memory system in the GA&CS to be recorded for processing.

1-12. Recording

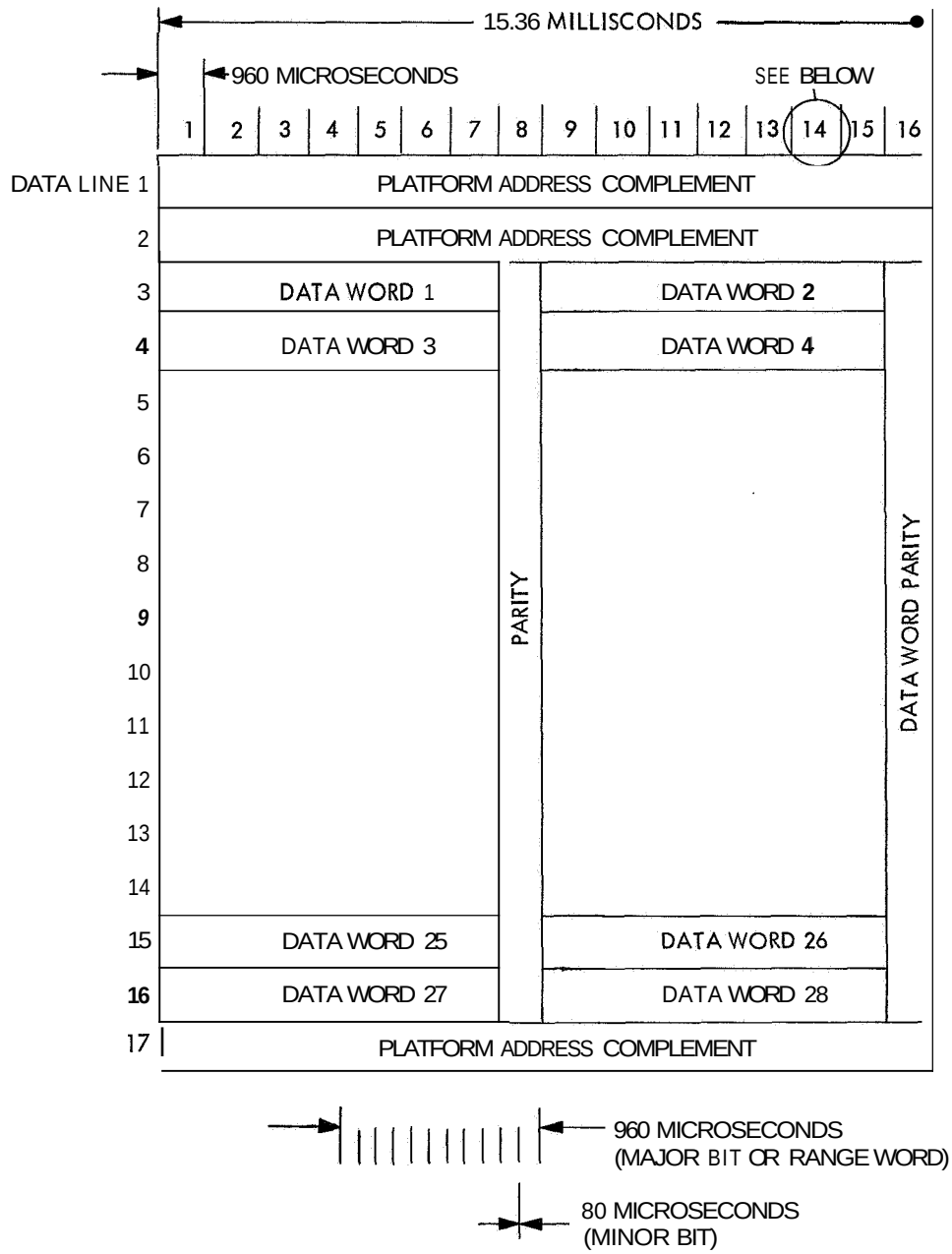
The data measured and encoded at the platform is transmitted to the IRLS satellite where it is stored in the data memory for subsequent readout to the GA&CS located in Fairbanks, Alaska or Rosman, North Carolina. The encoded data stored during any single orbit is a function of the number of platforms interrogated, the number of analog transducer sensing devices, and the resolution of the digitization at the platform. During each orbit, the IRLS satellite is capable of initiating *20* platform interrogation sequences. A total of 73 frames of data can be stored in the satellite data memory.

The storage of encoded data in the satellite data memory is accomplished by assembling the data at the platform in orderly frames of 272 bits each as shown in Figure 4. A single frame consists of three data lines of the address complement code and 28 data words of seven bits each. A standard platform is capable of transmitting either one or six data frames per satellite interrogation with each frame having up to 28 inputs from transducer sensing devices. The ISE is capable of being programmed to repeat a data frame one through six times. In addition to the data bits, each frame contains bit positions that contain partiy information when transmitted from the platform to the IRLS satellite. These vacant bit positions are utilized at the IRLS satellite for insertion of the ranging data and timing information necessary for the computation of the platform location.

The encoded data is transmitted digitally from the platform to the IRLS satellite at the rate of 1041 bits per second and loaded serially into the satellite data memory. The loading is controlled by synchronizing signals developed in the satellite digital circuits. When all data frames from the platform are received and loaded into the data memory, the memory loading process in the IRLS satellite is terminated. Platform transmission to the IRLS satellite ceases after the last data frame has been transmitted and the IRLS satellite proceeds to the next interrogation command word cycle at the end of 3.0 seconds.

At the completion of a programmed satellite interrogation sequence, the Nimbus Command and Data Acquisition (CDA) station, located at the same site as the GA&CS, transmits a command to the IRLS satellite for the readout of all data stored during the satellite-to-platform sequences. Data transfer from the IRLS satellite to the GA&CS is accomplished through the Nimbus spacecraft command system. When it is established that the communication link between the GA&CS and IRLS satellite is operating satisfactorily, a 16-bit GA&CS address code is transmitted to the IRLS satellite through the IRLS UHF channel signaling the commencement of data transfer. Data transfer is accomplished at the rate of 1041 bits per second until the entire contents of the 20,000 bit memory has been read out. Figure 5 illustrates data frame structure for transmission of stored encoded data and ranging information from the IRLS satellite to the GA&CS. A single frame consists of a data line comprised of a barker code for synchronization, a data line of the platform address complement code for synchronization, a data line of the platform address complement code for recognition, 28 data words of seven bits each, and two data words containing the range time code. In addition to the data bits, each frame contains bit positions that contain parity and range code information which determines the location of that particular platform.

After completion of data readout, the IRLS satellite is ready and capable of accepting new interrogation command words from the GA&CS that will determine the platform interrogation sequence of the next orbit, Figure 6A shows the information content of the format transmitted to the satellite command memory in order to program the IRLS satellite to interrogate up to 20 unmanned data stations. The transmitted information consists of one GA&CS address code and interrogation command time for individual platforms.

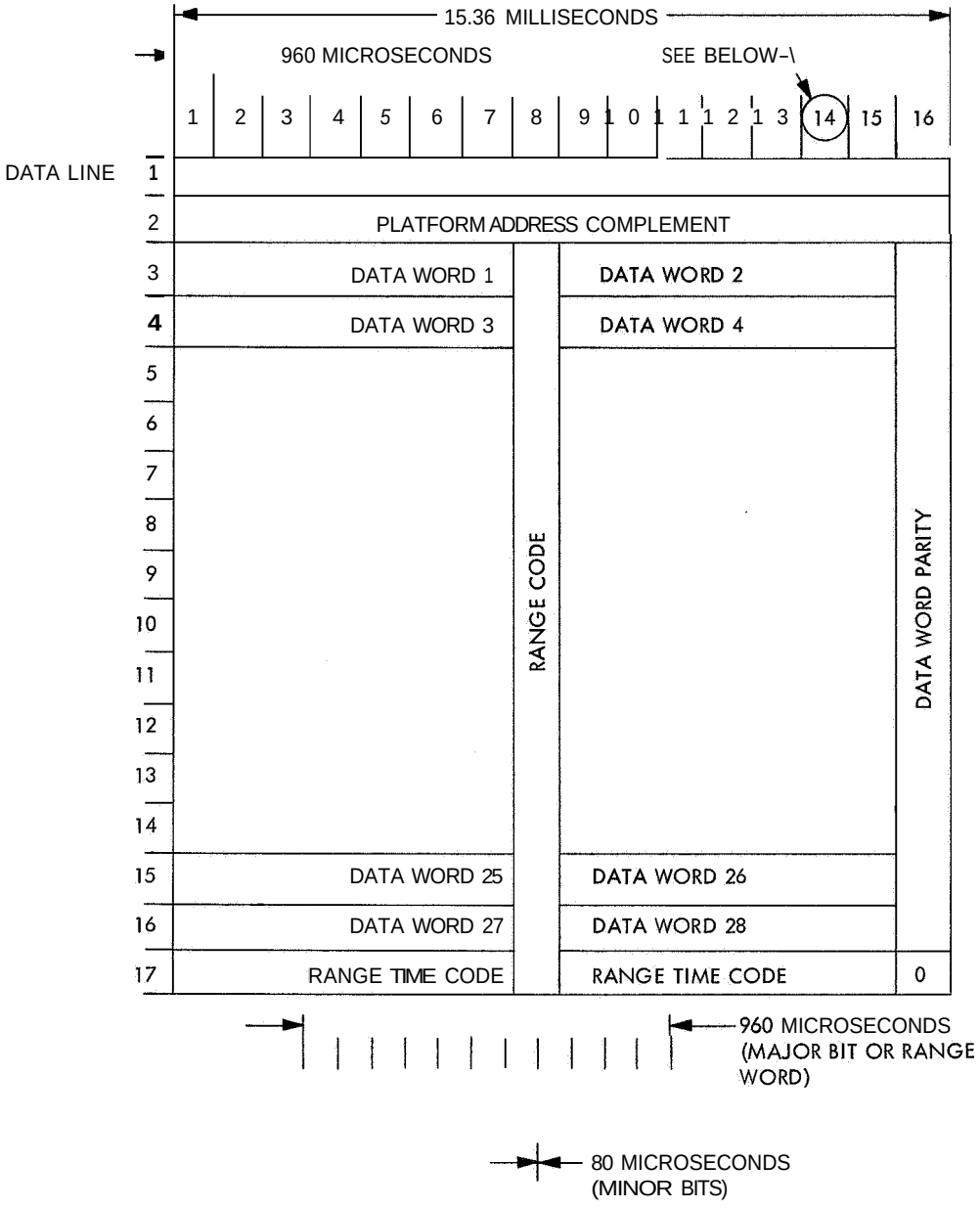


PLATFORM ADDRESS = 16 RANGE WORDS
DATA WORD = 7 RANGE WORDS, LSB FIRST
RANGE WORD
(MAJOR BIT) = 12 MINOR BITS (960 MICROSECONDS)
MINOR BIT = 80 MICROSECONDS
RANGE WORD = 8 MINOR BIT M-WORD FOLLOWED BY 4 MINOR BIT N-WORD

IF RANGE WORD VALUE IS ONE, THEN MINOR BIT VALUE OF M-WORD IS 10101100
IF RANGE WORD VALUE IS ZERO, THEN MINOR BIT VALUE OF M-WORD IS 01010011
FIRST N-WORD OF EACH DATA WORD LINE HAS MINOR BIT VALUES OF 0110
REMAINING 15 N-WORDS OF EACH DATA WORD LINE HAVE MINOR BIT VALUES OF 1001

55369

Figure 4. Platform-to-Satellite Data Frame Structure.



BARKER CODE	=	16 RANGE WORDS
PLATFORM ADDRESS	=	16 RANGE WORDS
DATA WORD	=	7 RANGE WORDS, LSB FIRST
RANGE TIME CODE	=	7 RANGE WORDS
RANGE WORD (MAJOR BIT)	=	12 MINOR BITS (960 MICROSECONDS)
MINOR BIT	=	80 MICROSECONDS
RANGE WORD	=	8-MINOR BIT M-WORD FOLLOWED BY 4-MINOR BIT N-WORD

IF RANGE WORD VALUE IS ONE, THEN MINOR BIT VALUE OF M-WORD IS 10101100

IF RANGE WORD VALUE IS ZERO, THEN MINOR BIT VALUE OF M-WORD IS 01010011

FIRST N-WORD OF EACH DATA WORD LINE HAS MINOR BIT VALUES OF 0110

REMAINING 15 N-WORDS OF EACH DATA WORD LINE HAVE MINOR BIT VALUES OF 1001

56739

Figure 5. Satellite-to-GA&CS Data Frame Structure.

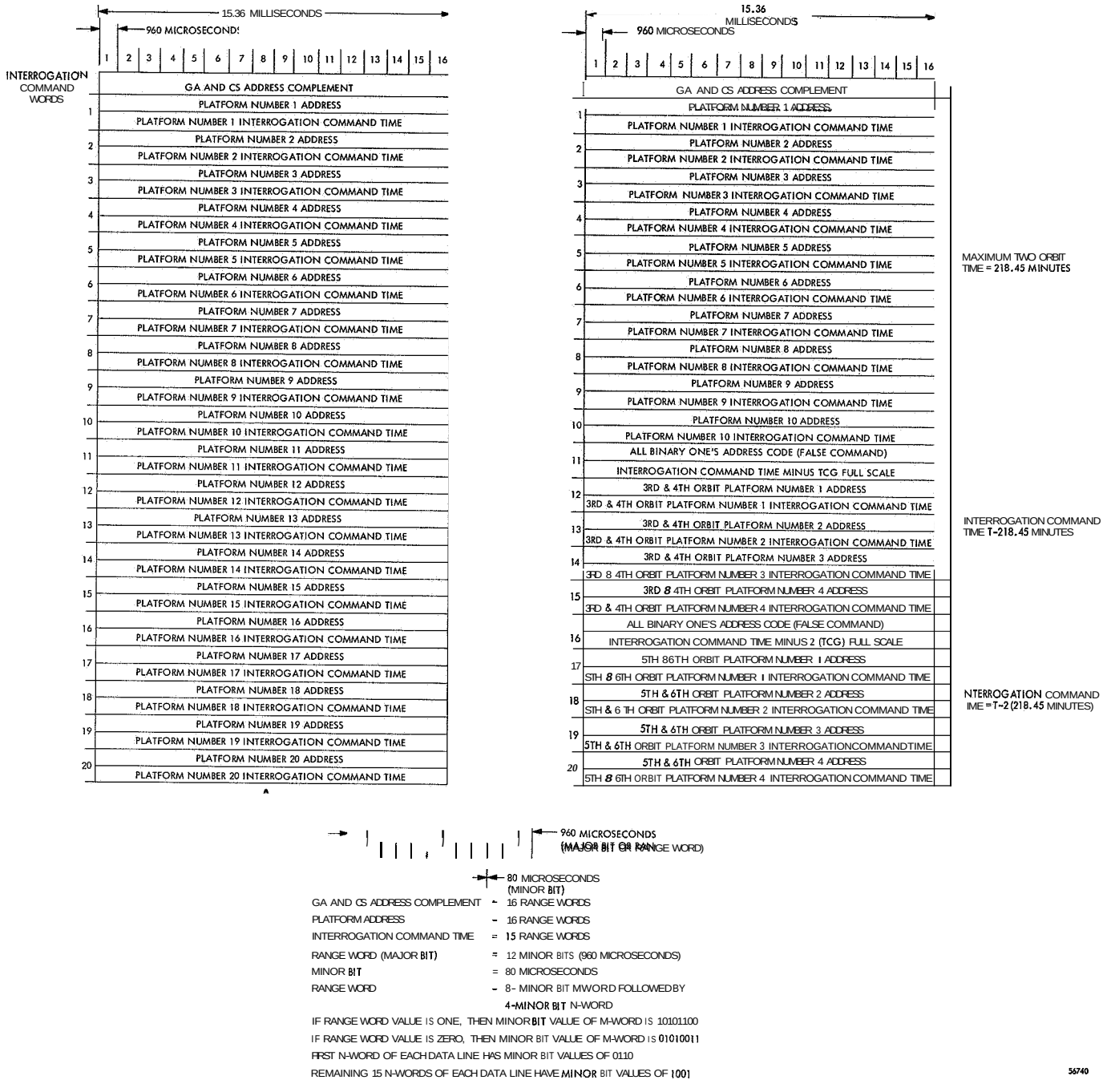


Figure 6. GA&CS-to-Satellite Interrogation Command Word Structure.

After the input data is received and stored in the data memory of the GA&CS, additional processing is required to separate the data frames. This is accomplished by a data processor in the GA&CS that sorts out data frames and assembles the data into a suitable format for distribution to the appropriate agency. This output format consists of each platform's identification address, decoded data, time of interrogation, and additional data developed by the IRLS satellite that enables platform location to be computed. Figure 6B shows a typical information content of the format transmitted to the satellite command memory to allow the IRLS satellite to interrogate platforms without being commanded at the end of each orbit by the GA&CS. The information content is comprised of one GA&CS address complement for recognition and then alternate transmissions of the platform address code and interrogation command time for selected platforms during an elapsed time required for two orbit. (maximum of 218.45 minutes). The next command depicted by Figure 6B is an all binary ONE's false command inserted in order to allow the time code counter in the IRLS satellite time code generator to transit from full scale to zero, The following interrogation command times are represented by T-218.45 minutes for the maximum elapsed time required for orbits, The address codes for the selected platforms are transmitted in a normal manner. If more than four orbits are required, the false ONE's command is again repeated and the interrogation command time is represented by T-2 (218.45) minutes.

1-13. Location

The location of each platform, in terms of latitude and logitudinal coordinates, is determined by using the geometrical relationship that exists between the IRLS satellite and platform which yields a mathematical solution when the distances between the two units are known. The IRLS provides the distance information by a range measurement technique described in paragraph 1- 20.

Platform location is derived from multiple measurements of the distance between the IRLS satellite and platform and using these measurements in a geometrical equation. This geometry is shown in Figure 7. Computer analysis has shown that two measurements of the distance R1 and R2 are all that is required to establish platform location. The two range measurements (distance) and the chord distance the IRLS satellite travels between measurements R1 and R2 defines a plane triangle in space, intercepting the earth at the platform. Since the IRLS satellite ephemeris is known, all sides of the triangle can be determined. In the IRLS, the exact time of each range measurement is recorded which, together with the IRLS satellite orbital parameters, allows the third side of the plane triangle to be calculated. The vertical projection of this triangle onto the earth's surface defines a spherical triangle having as its vertices, the subsatellite points SS1 and SS2 along the ground track and the platform.

Once this construction is complete and the coordinates of the subsatellite points are computed from the ephemeris data, platform latitude and longitude can be computed,

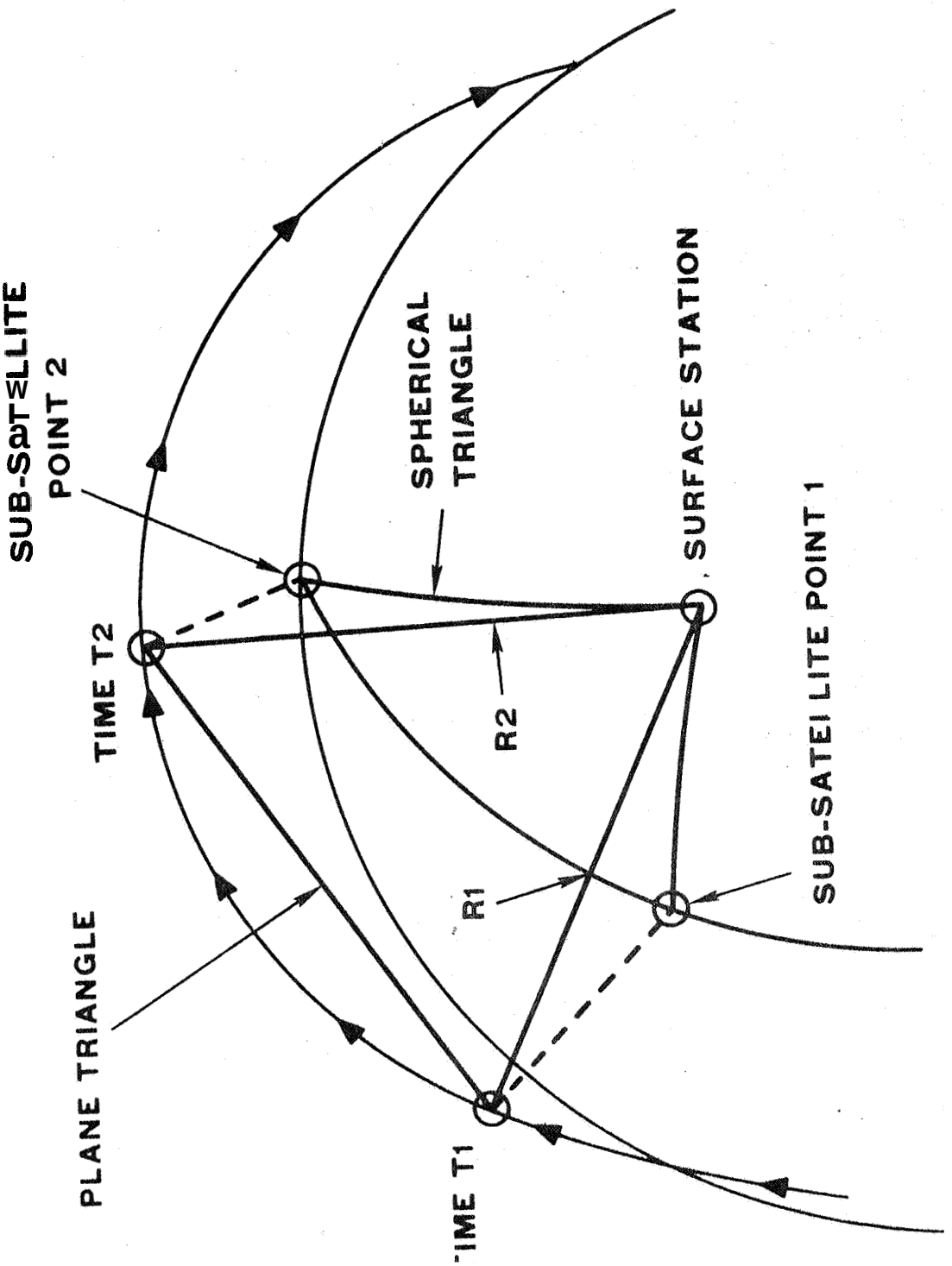


Figure 7. Platform Positioning Geometry.

1-14, MAJOR CHARACTERISTICS.

1-15. General.

The following paragraphs provide information and descriptions of functions and signal structures necessary to the understanding of operational sequences and data generation performed between the maior equipment components to the IRL Subsystem. These discussions pertain primarily to the major characteristics of the overall IRL Subsystem.

1-16. Signal Structure.

The structural pattern utilized in formulating data bit trains and data words in the communication sequence between the IRLS satellite, platform, ISE, and GA&CS equipment is the range word sequence. This sequence is a set of 192 non-return-to zero (NRZ) bits corresponding to 16 range words comprised of 12 bits each that are generated at a 12.5 kilobit rate. Each 80-microsecond duration bit of the sequence is called a minor bit and 12 minor bits comprise a range word. There are 16 range words, each divided into two distinct parts. The first eight minor bits comprise the. M-word and minor bits 9 through 12 make up the N-word. Each range word in a datu frame or communication sequence is transmitted at a 1.04 KB rate and represents a binary number called a major bit. Each 12 minor bit sequence necessary to generate one major bit has a total bit length of 960 microseconds. Range word information is transmitted at the 1.04 KB rate by inverting or not inverting the eight minor bit M-word of each 12-minor bit range word pattern. Synchronization and platform-to-satellite range computation is facilitated by inverting the four minor bit N-word once during every 16 range words. The 1.04 KB range word transmission rate is derived from the fact that it takes 960 microseconds to transmit the twelve 80-microsecond wide minor bits that comprise one range word. Thus, each range word is transmitted at the rate of 1.04 KB (1000 divided by 960) or one range word data bit per millisecond.

For purposes of identification, each group of 12 minor bits is assigned a range word number n to describe its location within the sequence, where, n equals range word 1 through 16. Also, each minor bit of the range word is assigned a number k to locate its position in the word, where k equals minor bits 1 through 12. If b^n is a binary variable representing a range word value ($b \equiv$ binary ZERO or $\overline{b} \equiv$ binary ONE), then b^n_k is the value of the k^{th} minor bit in the n^{th} range word. Thus, the n^{th} range word could be written .

$$b^n_1 b^n_2 b^n_3 b^n_4 b^n_5 b^n_6 b^n_7 b^n_8 b^n_9 b^n_{10} b^n_{11} b^n_{12}$$

Range word minor bits k 1 through k 8 are used to represent the maior bit (range word) value, These eight bits comprise the M-word. If the major bit value is a binary ONE, then the minor bits in the M-word are 10101100 and called the reference M-word or "M". If the major bit value is binary ZERO, the minor bit M-word is the complement of the reference M-word, $\overline{M}$, or 01010011.

Range word minor bits k 9 through K12 are used to synchronize the range word sequency. These four minor bits comprise the N-word and are 1001 for range words n 2 through n 16. The first range word in each 16-range word sequency has the N-word complement value of 0110 or $\overline{N}$.

The time sequence of minor bit transmission is, as time increases;

$$b_1^1 b_2^1 \text{----} b_{12}^1,\ b_1^2,\ b_2^2 \text{-----} b_{12}^{16},\ b_1^1$$

With exception of the 15 bit interrogation command time, all platform and GA&CS address and data transmission is in groups of 16 major bits. These major bits are coherent with the 16-word range sequence. The leading edge of minor bit b_1^1 and trailing edge of b_{12}^1 encompasses the first major bit of any 16 bit data group, The leading edges of bits $b_1^1, b_1^2, b_1^3, \text{-----} b_1^{16}$, represent divisions that separate major bit NRZ data.

1-17. Synchronization and Detection.

The output from the platform receiver is regenerated as an NRZ signal in the PCM demodulator and bit synchronizer. A regenerated range word sequence consisting of 12.5 KB data is derived from this NRZ signal and utilized in the sync demodulator and correlator to generate synchronization signals.

The regenerated range word sequence is synchronized (phased-locked) with the receiver output 12.5 KB bit frequency. The regenerated range word sequence is comprised entirely of reference M-words and the corresponding N-words and is utilized in the development of synchronization pulses in the following manner,

The most recent twelve minor bits of the regenerated range word sequence are examined to generate synchronizing signals. This set of minor bit values can be represented as $a_0 a_{-1} a_{-2} \text{-----} a_{-11}$ where a_0 is the most recent bit. If $a_0 a_{-1} a_{-2} a_{-3}$ is 1001 or 0110 and if $a_{-4} a_{-5} a_{-6} a_{-7} a_{-8} a_{-9} a_{-10} a_{-11}$ is 00110101 or 11001010, then it is assumed that $a_0 = b_{12}^n$, $a_{-1} = b_{12}^n$, etc., where n equals range words one through 16 and word synchronization is achieved. Whenever $a_0 a_{-1} a_{-2} a_{-3}$ is 0110 and $a_{-4} a_{-5} a_{-6} a_{-7} a_{-8} a_{-9} a_{-10} a_{-11}$ is 00110101 or 11001010, then it is assumed that a_0 is the value of minor bit 12 in range word one and pattern synchronization has been achieved.

If phase lock is not achieved in the platform bit synchronizer before occurrence of the platform address sync pulse, a logic ZERO error threshold level from the bit synchronizer inhibits data frame generation. The address sync pulse applies a preset voltage to the last stage of the platform address register and digital multiplexer causing the output of that stage to remain at a constant logic ONE level.

This results in the generation of a modulated data stream of repeated logic ONE's until phase lock (synchronization) between the receiver output and the regenerated range word sequence in the synchronizer. When this occurs, the error threshold output from the bit synchronizer attains a logic ONE level, indicating that phase lock has been achieved, and removes the preset voltage from the platform address register and digital multiplexer and initiates data frame transmission.

1.18. Data Handling.

The 16-range word digital sequence is utilized as the RF carrier modulation signal for all transmissions between the satellite, platform, ISE, and GA&CS. For transmission of PCM telemetry signals, the sequence also serves as a digital subcarrier that is further modulated to represent the data.

Data modulation is accomplished by operating upon the 8-minor bit M-word of each 12-minor bit range word. A range word value of ONE is represented by the M-word bit pattern 10101100, and a range word value of ZERO is represented by the M-word complement or 01010011.

The digital data that modulates the 12.5 KB digital subcarrier must be synchronized and at a frequency of 1.04 KB which is the repetition rate of M-words. The modulation must be inhibited during the period of time of the N-word, which is the last 320 microseconds (four minor bit times) of each of the 16 range words so that the N-word is not modulated.

Demodulation of the modulated subcarrier after RF transmission is accomplished with the aid of an unmodulated reference signal that is comprised of the M-word complement in synchronism with the received modulated 12.5 KB subcarrier. This signal is generated by using the unmodulated N-words that are received from the RF link as synchronizing data to allow regeneration of the range word sequence. As previously discussed, a phase-lock operation in the bit synchronizer provides synchronization of the regenerated range word sequence with the received 12.5 KB phase and frequency.

1.19 Platform Acquisition.

Acquisition of a platform requires identification and timing synchronization before data transfer can be initiated. Identification and verification of synchronization are accomplished through the use of a platform address code comprised of 16 range words. Each platform is assigned its own discrete digitally-coded 16-range word address which is hardwired in the address and address correlators. The arrangement of address code words is specified in such a manner that the address of each platform differs from all others in at least three words, contains at least three logic ONE values, is not the complement of another platform address, GA&CS address, or barker word, and is not cyclic. This assures maximum security against wrong platform response to a satellite interrogation.

The IRLS satellite, when the stored interrogation command time in the command memory is coincidence with elapsed orbit time, transmits the stored platform address code contents of the command memory as a 1.04 KB modulation of the 12.5 KB range word sequence. On reception of the transmitted address, the platform regenerates the range word sequence and performs a correlation between this sequence and a hardwired address code in the address and address correlators. If correlation between the transmitted address and hardwired address is achieved, the platform retransmits the address back to the IRLS satellite.

Reception of the address code by the IRLS satellite indicates that the platform is operating and capable of communication. The IRLS satellite verifies that the platform address code contents of the command memory is identical to the received address code, achieves phase synchronization with the received address code, and transmits the address complement (address) back to the platform. When the address code is recognized by the platform, data

frame generation is initiated provided phase synchronization between the receiver input and the regenerated 12.5 KB data has been achieved in the PCM demodulator and bit synchronizer. With minor exceptions, the IRLS satellite-to-GA&CS acquisition sequence is accomplished in an identical manner. The exception being that the GA&CS address code transmission from the satellite is compared and verified with a GA&CS address code stored in the GA&CS digital data processor.

1-20. Ranging.

The distance between the IRLS satellite and a platform is measured by determining propagation time of the RF signal. The IRLS satellite modulates its RF carrier with the range word sequence. The platform receives this input and retransmits it back to the IRLS satellite. The IRLS satellite determines the time shift between received and transmitted sequences, a quantity that is directly related to distance by the propagation velocity of approximately 0.162 nautical mile per microsecond. A binary-coded number, representing the measured propagation delay time, is stored by the IRLS satellite for later transfer to the GA&CS with the encoded platform data.

The binary-coded range number is developed by counting the cycles of a 1.6-mcps clock output from the Nimbus spacecraft as follows. When a platform address complement is recognized by the IRLS satellite and phase-lock of the satellite bit synchronizer is complete, the counter in the satellite range detector is permitted to count 1.6-mc transitions. When the corresponding point in the sequence being generated and transmitted by the IRLS satellite is reached, the range detector counter ceases operation. The generated count code is a representation of the total communications link propagation delay including fixed delays in the IRLS satellite and the platform. The code count can be readily converted to a one-way range by the formula shown in Figure 8. As shown on the illustration, the one-way range may be calculated in either nautical miles or kilometers in relationship with the range code. Due to the complex nature of the propagationvelocity, the constant K is an approximation. An exact propagation constant may be calculated by knowing the index of refraction of the troposphere, the ionosphere, and the attack angle. In the event that the computed one-way range is less than the orbital altitude, it is necessary to add 1065.17 nautical miles or 1972.6 kilometers to the range to compute the actual one-way range.

1-21. Satellite and Platform Time Delays.

The IRLS satellite and platform have an inherent time delay of approximately 1.10 milliseconds. This time delay is an accumulaton of microsecond delays through the functional logic and receiver circuits and varies with individual units of equipment. Inherent delay information will be forwarded to the user agency prior to equipment utilization.

1-22, Redundant Transmitter Turnoff and Operational Modes.

Provision is incorporated into the IRLS satellite to deenergize the transmitter if the communication link between the IRLS satellite and GA&CS or platform cannot be satisfied and data transfer cannot be accomplished. During the satellite-to GA&CS sequence, this event would occur after the transmitter is energized due to reception of a spacecraft turn-on command from the CDA. Coincident with turn-an, the time code generator in the IRLS

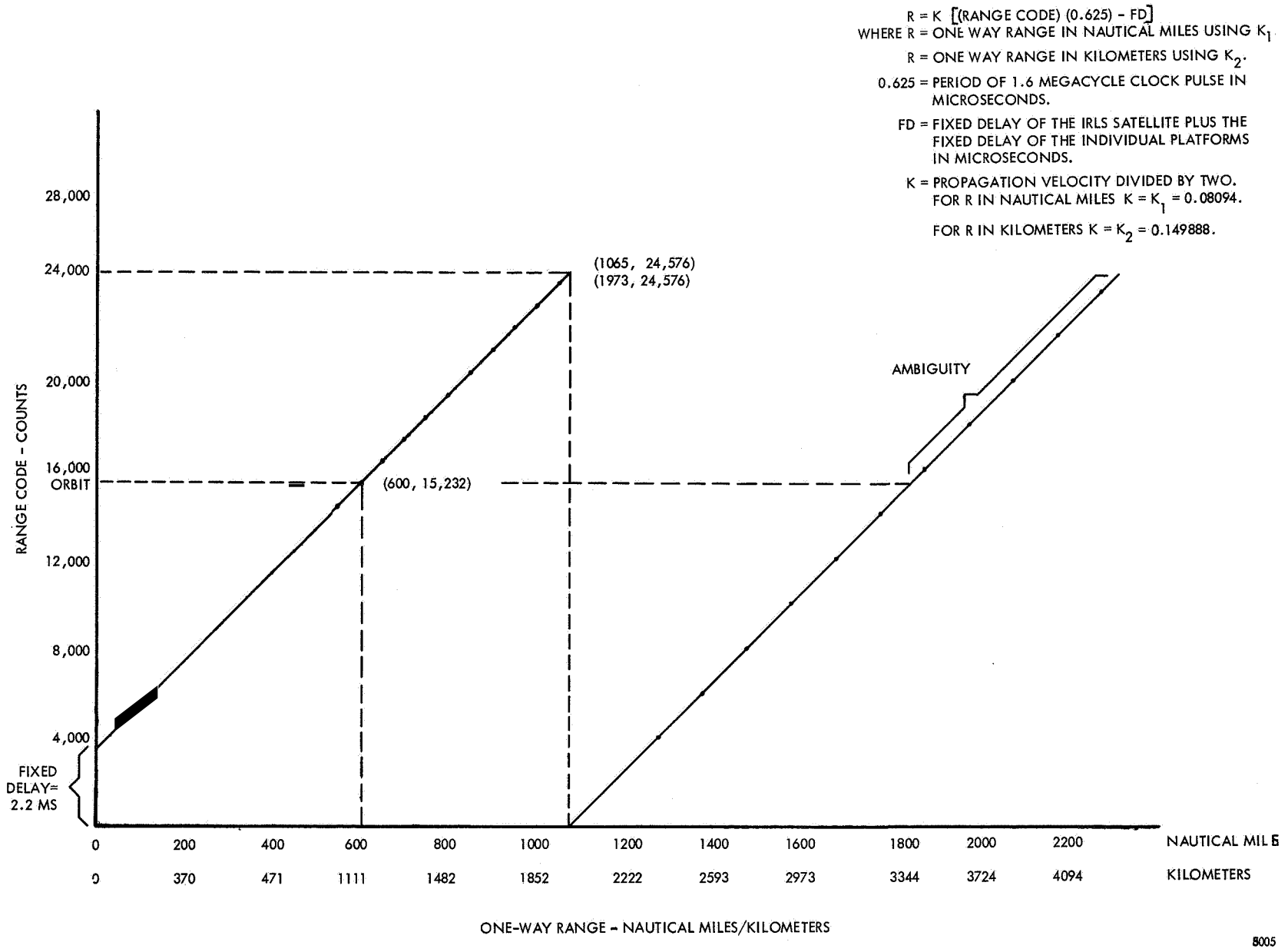


Figure 8. Satellite-to-Platform One-Way Range.

satellite is reset which, in turn, starts a 10-second elapsed time counter. After 10 seconds, the GA&CS address decoding and verification process is sampled to detect verification. If the address code cannot be decoded due to bad input data or a malfunction, a turn-off command automatically deenergizes the transmitter.

During the satellite-to-platform sequence, this event would occur after the satellite transmitter is energized due to time coincidence between the interrogation command time stored in the satellite command memory and the IRLS elapsed time. Coincident with transmitter turn-on, a three second counter is enabled which, at the end of 3.0 seconds maximum, generates a transmitter turn-off command. This operation does not involve recognition of the platform address or address code patterns and is independent of data. reception.

Provision is also incorporated into the platform to deenergize the transmitter if data frame transmission is not completed. This event would occur if the transmitter were energized due to recognition of a platform address and it did not recognize an address complement. As in the satellite, coincident with turn-on, a three-second counter is also enabled which, at the end of 3.0 seconds maximum, generates a transmitter turn-off signal.

Generally, the platform transmitter in the ISE is essentially a passive instrument that the telemetry transmitter is normally in a continuous standby operational mode. During this mode, the filaments of the transmitter power amplifier output tube remain energized to assure a transmitter turn-on time of less than 100 milliseconds when a transmitter ON command places the platform equipment in an operational mode. In order to prevent damage to the telemetry transmitter, a minimum warmup time of 120 seconds is required prior to application of a transmitter ON command. The transmitter ON command is derived from detection of the correct platform address code as received from satellite transmission. The platform equipment functions in the operational mode for a maximum of 3.2 seconds or until one platform interrogation sequence is terminated, whichever is shorter. At this time, a transmitter OFF command is initiated which returns the platform equipment to its standby operational mode. The telemetry receiver operates continuously to provide uninterrupted monitoring for transmission of address codes to initiate another interrogation.

1-23. Blind Orbit Capability.

The blind orbit capability of the IRL Subsystem is defined as the capability of the IRLS satellite to perform platform interrogation sequences without reception of commands from the GA&CS over a predetermined number of orbits. In order to accomplish this action, the satellite command memory must receive appropriate platform address codes and interrogation command times from the GA&CS (Figure 6B) during a GA&CS-to-satellite interrogation sequence. Programming the command memory for the reasons described in the following paragraphs allows the maximum elapsed time capability (218.45 minutes) of the satellite time code generator to be extended to compensate for additional orbits.

The time code generator in the satellite data and ranging module is capable of counting elapsed time to a maximum of 218.45 minutes. With this restriction and using a nominal one-orbit time of 107 minutes, the maximum number or orbits allotted within the

capability of the time code generator is two with 4.45 minutes allotted for slight deviations. Generation of a time coincidence between the interrogation command time from the satellite command memory and the elapsed time in the time code generator initiates each platform interrogation sequence. Thus, if the maximum two-orbit time capability is to be overrun, it is possible to program the command memory to permit a greater number of orbits by insertion of a false 16-bit command and insertion of an interrogation command time represented by T-218.45 minutes.

Programmed interrogation command times greater than the maximum two-orbit time of 218.45 minutes are represented by T-218.45 minutes while commands representimg times greater than the maximum four-orbit time of 2(218.45 minutes) is represented by T-2(218.45) minutes. As previously mentioned, the time of 218.45 minutes is the full count of the time code generator. Thus, in order to utilize the additional orbit capabilities of the time code generator after a transition from full-scale-to zero, it is necessary to insert a false command of all binary ONE's (full-scale) in the command memory prior to the first valid interrogation command time that exceeds 218.45 minutes. Therefore, it is possible to extend the capability of the satellite time code generator tofunction for as many orbits as required if the following procedure is utilized.

a. Base all programmed interrogation command times on the termination of the satellite data memory READ mode.

b. If the interrogation command time is greater than the elapsed time required for two orbits (218.45 minutes or full scale of the time code generator), program T-218.45 minutes in the 16-bit portion of the 32-bit interrogation command word transmitted to the IRLS Satellite.

c. In order for the time code generator to recognize T-218.45 minutes, insert a false command of all binary ONE's immediately proceeding the first interrogation command time exceeding 218.45 minutes.

d. If an interrogation command time is greater than the elapsed time required for four orbits 2(218.45 minutes) or two cycles of the time code generator, program T-2(218.45) minutes in the 16-bit portion of the 32-bit interrogation command word, preceeded by false 16-bit word command of all binary ONE's.

e. In all cases, no interrogation command time will be greater in magnitude than 13,100 seconds, except for the full-scale false command immediately preceeding the 16-bit time command.

SECTION II

FUNCTION AND

PHYSICAL DESCRIPTION

2-0. FUNCTION AND PHYSICAL, DESCRIPTION.

2-1, ISE FUNCTION.

The primary objective of the Integration Support Equipment is to provide a method of monitoring IRLS satellite operation for proper functional capabilities and correct operating parameters prior to incbrporating the satellite into the Nimbus Spacecraft or immediately prior to launch during preflight checks of the launch vehicle. A secondary, but not in the least unimportant, objective of the ISE is to provide a removable and easily-handled self-test facility for operation verification of the IRLS platform equipment during field installation or field maintenance. The ISE implements these objectives by having the capability of functioning in three similar modes of operation. Each mode is self sufficient and capable of performing its assigned task with a high degree of reliability. With proper switch programming, the first mode allows the ISE to function with the satellite transmitter output connected directly to the ANTENNA PORT connector located on the rear panel of RF control 1A6. The correct positioning (30 DB) of the INITIAL ATTENUATION switch on the front of RF control 1A6 permits attentuation of RF power from both the ISE and satellite transmitters by inserting two fixed 15 db power attenuators and a 0-109 low-power variable attenuator into the signal path.

With a GFE loop-vee, crossed dipole, or other antenna configuration complying with performance requirements connected to the ANTENNA PORT connector, this mode also facilitates operational checkout of a satellite in close proximity to the ISE. As previously mentioned, the close proximity checkout is usually accomplished during preflight checks of the launch vehicle. The second mode is the normal satellite-to-platform interrogation sequence, via the transmission link, thatisperformed as the IRLS satellite orbits the earth aboard the Nimbus Spacecraft. Proper programming of the front-panel switches on the ISE is also necessary for this mode. The third mode is the self-check mode in which the ISE determines, on a GO/NO GO basis, the operational capability of the IRLS platform mounted in RF control 1A6 or any other IRLS platform. This mode must also be programmed by repositioning front-panel switches on analog control 1A4, self-check 1A5, and RF control 1A6. In performance of the self-check, the ISE verifies that the platform transmits a correct address code, that it transmits three address complements per data frame, that the data words (including parity) are correct according to a preselected code, and that the correct number of data frames are transmitted. Verification of these parameters results in a GO indication on self-check 1A5 while a malfunction in any one parameter causes a NO GO indication.

2-2. PHYSICAL DESCRIPTION.

2-3. General.

The Integration Support Equipment system is a self contained test unit mounted in a movable electrical equipment cabinet containing a standard 19-inch equipment rack. The equipment cabinet housing the system components is 78.5 inches high, 25 inches wide, 25.5 inches deep, and mounted on 3.5-inch casters for portability. Each cabinet contains the ISE platform, self-check electronics, and the standard test equipment necessary to maintain the ISE and provide the necessary functional tests to confirm proper operation of the IRLS. A utility storage drawer, a retractable writing surface, and a blower to maintain ambient

temperature within the cabinet are also provided. Access to the rear of the system subassemblies is gained through a full length rear door.

The two system configurations are illustrated in Figure 9 and Figure 10. System 1 is identical to Systems 2 and 3 with the exception of a digital counter (1A1) included in System 1 (517532-G1) only. The remaining equipment contained in each ISE rack are power meter and voltmeter 1A2, IRLS time delay simulator 1A3, analog control panel 1A4, self-check assembly 1A5, RF control unit containing the ISE platform 1A6, recorder 1A7, power supply 1A8, centrifugal fan 1A9, and AC distribution panel 1A10. The AC distribution panel is located in the rear of the cabinet behind the meter rack adapter 1A2. Drawer type chassis are mounted from the front and rest on nylon covered angle mounting brackets within the cabinet. All units are then secured to the rack with phillips-head machine screws through their respective front panels. Semipermanent interface and power connections are made at the rear of the system via the access door. A slotted wire duct is provided on the left-hand side within the cabinet for all intrarack wiring and cabling, and an AC power strip (1A11) is located on the right-hand side for all equipment power connections. Detailed physical characteristics are summarized in Table 1. The following paragraphs describe the physical characteristics of Radiation-built subassemblies contained in the ISE. This equipment includes the IRLS platform contained in the RF control unit, analog control panel 1A4, self-check unit 1A5, RF control unit 1A6, and AC distribution panel 1A10. Standard test equipment included in the system is mounted in rack adapters where necessary to fit the 19-inch equipment rack. The standard equipment are the following:

a. Electronic Counter HP5245L (517532-G1 Configuration only) - 1A1

b. Electronic Voltmeter HP410C and Power Meter HP431C - 1A2

c. Event Recorder, Sanborn Model 361 - 1A7

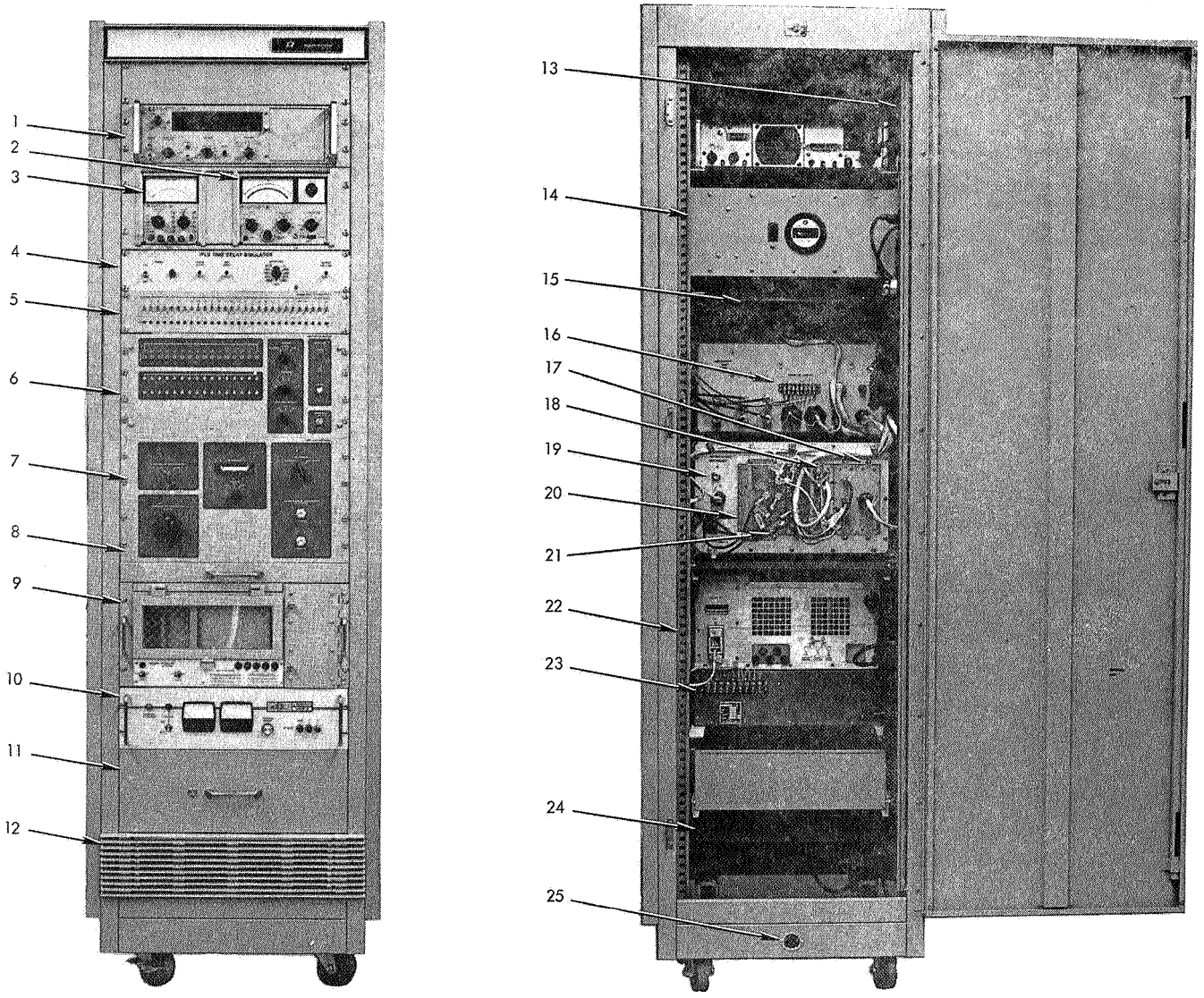
d. Power Supply, Sorensen Model QB28-8 - 1A8

Physical and electrical characteristics are fully described in the individual manufacturers' equipment manuals supplied with the system. Any unequipped sections of the ISE are fitted with appropriate blank panels to completely enclose the system and provide a finished appearance to the front of the system.

2-4. ISE Platform.

2-5. General.

The ISE platform is located within RF control unit 1A6 and comprises four modules: PCM/FM UHF transmitter/diplexer module A1, PCM/FM UHF receiver module A2, data and ranging module A3, and power control and distribution module A4. The modules are mounted on the rear panel of the RF control unit and extend into the unit. Access to the four modules is gained through the rear access door of the system cabinet. Opening the door exposes the mounting sides and cable connectors of the modules. Mounting arrangements for the modules position transmitter/diplexer module A1 in the extreme left position of the



1. Electronic Counter 1A1
2. Electronic Voltmeter 1A2
3. RF Power Meter 1A2
4. IRLS Time Delay Simulator 1A3
5. Analog Control 1A4
6. Self Check 1A5
7. RF Control 1A6
8. Writing Surface
9. Event Recorder 1A7
10. Power Supply 1A8
11. Storage Drawer
12. Blower 1A9
13. AC Power Strip
14. AC Distribution 1A10
15. Analog Control Terminal Board 1A3TB1
16. Self Check Terminal Board 1A5TB1
17. Data and Ranging 1A6A3
18. Power Control and Distribution 1A6A4
19. ANTENNA PORT Connector 1A6J4
20. Transmitter/Diplexer 1A6A1
21. Receiver 1A6A2
22. DC Power Cabling
23. Power Supply Terminal Board 1A8TB1
24. Blower 1A9
25. Primary Power Connector 1J1

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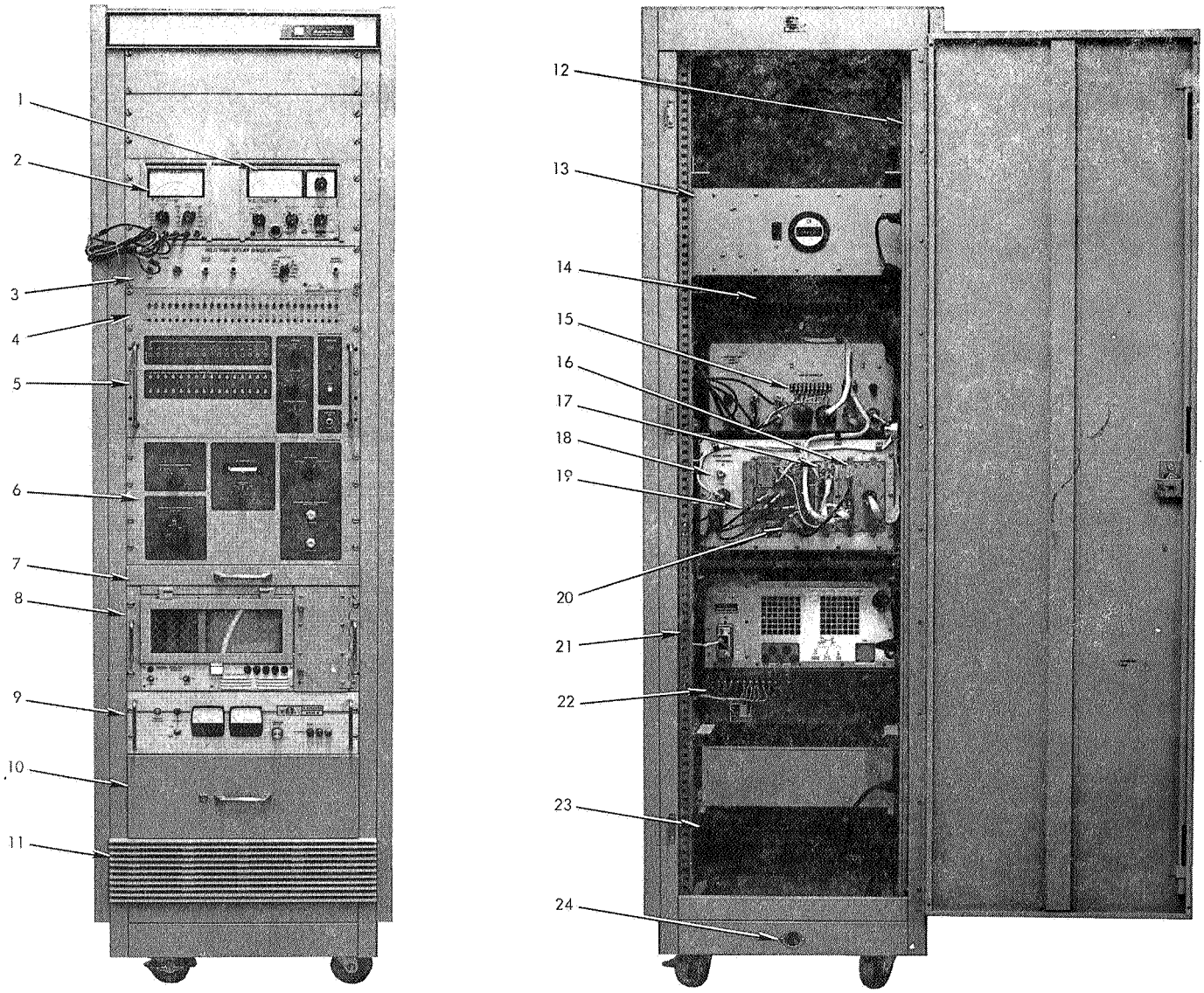
Figure 9. Integration Support Equipment 517532-G1, Front and Rear Views.



1. ticctronic Voltmeter *1P2*
2. RF Power Meter 1A2
3. IRLS Time Delay Simulator 1A3
4. Analog Control 1A4
5. Self Check 1A5
6. RF Control 1A6
7. Writing Surface
8. Event Recorder 1A7
9. Power Supply 1A8
10. Storage Drawer.
11. Blower 1A9
12. AC Power Strip
13. AC Distribution 1A10
14. Analog Control Terminal Board 1A3TB1
15. Self Check Terminal Board 1A5TB1
16. Data and Ranging 1A6A3
17. Powsr Control and Distribution 1A6A4
18. ANTENNA PORT connector 1A6J4
19. Transmitter/Diplexer 1A6A1
20. Receiver 1A6A2
21. DC Power Cabling
22. Power Supply Terminal Board 1A8TB1
23. Blower 1A9
24. Primary Power Connector 1J1

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Figure 10. Integration Support Equipment 517532-G2, Front and Rear Views.

Table 1. Physical Characteristics

Unit	Characteristics
Equipment Rack	Dimensions Height: 78-1/2 inches Width: 25 inches Depth: 25-1/2 inches Portability: 3-1/2 inch casters Finish Primer: Zinc chromate per MIL-P-8585 (ES 111-900024) Finish Coat: Enamel, lisht-gray, semigloss per TT-E-529, class B (ES 850034), color clip No. 26314
Electronic Counter 1A1 (517532-G1 Configuration Only)	Dimensions Height: 5-1/4 inches Width: 19 inches Depth: 16-1/2 inches Weight: 32 pounds (less Model 5253B Frequency Converter) Frequency Converter Weight: 5 pounds Environment: 25°C to 40°C at 50-95 percent relative humidity for five days
Electronic Voltmeter 1A2	Dimensions Height: 6-1/2 inches Width: 5-1/8 inches Depth: 11 inches Weight: 8 pounds
Power Meter 1A2	Dimensions Height: 6-3/32 inches Width: 7-25/32 inches Depth: 12 inches (including controls) Weight: 7 pounds

Table 1. Physical Characteristics (Continued)

Unit	characteristics
IRLS Time Delay Simulator 1A3	Dimensions Height: 3-1/2 inches Width: 17 inches (19 inches with front panel) Depth: 7 inches Finish Primer: Zinc chromate per MIL-P-8585 (ES1' 1-900024) Finish Coat: Enamel, light-gray, semigloss, per TT-E-529, color chip No. 26314.
Analog Control 1A4	Dimensions Height: 3-1/2 inches Width: 19 inches Depth: 1-1/2 inches Depth with cable connector: 4-1/2 inches
Self Check 1A5	Dimensions Height: 9 inches Width: 17 inches (19 inches with front panel) Depth: 12 inches Weight: Approximately 25 pounds. Finish Primer: Zinc chromate per MIL-P-8585 (ES111-900024) Finish Coat: Enamel, light-gray, semigloss, per TT-E-529, color chip 26314.
RF Control 1A6	Dimensions Height: 10-1/2 inches Width: 17 inches (19 inches with front panel) Depth: 19-1/2 inches

Table 1. Physical Characteristics (Continued)

Unit	Characteristics
RF Control 1A6 (Continued)	Finish Primer: Zinc chromate per MIL-P-8585 (ES 111-900024) Finish Coat: Enamel, light-gray, semigloss per TT-E-529, color chip 26314.
Transmitter/Diplexer 1A6A1	Dimensions Height: 4 inches Width: 6 inches Depth: 6-1/2 inches Weight: 7 pounds Construction: Aluminum Finish: Electroless nickel
Receiver 1A6A2	Dimensions Height: 2 inches Width: 6 inches Depth: 6-1/2 inches Weight: 2.5 pounds Construction: Aluminum Finish: Electroless nickel
Data and Ranging 1A6A3	Dimensions Height: 4 inches Width: 6 inches Depth: 6-1/2 inches Weight: 4.0 pounds Construction: Chromate treated aluminum

Table 1. Physical Characteristics (Continued)

Unit	Characteristics
Power Control and Distribution 1A6 A4	Dimensions Height: 2 inches Width: 6 inches Depth: 6-1/2 inches Weight: 2.9 pounds Construction: Chromate treated aluminum
Writing Surface	Dimensions Height: 2 inches Width: 19 inches Depth: 21 inches
Event Recorder 1A7	Dimensions Height: 8-3/4 inches Width: 19 inches Depth: 14-1/2 inches (15-1/4 inches including controls) Environment: 0°C to 50°C
Storage Drawer	Dimensions Height: 7 inches Width: 19 inches Depth: 18-3/4 inches
Centrifugal Fan 1A9	Dimensions Height: 5-1/4 inches Width: 19 inches Depth: 7 inches Bearings: Ball Finish Housing: Gray hammertone enamel over zinc-chromate primer Grill: Chrome-plated cold-rolled steel

Table 1. Physical Characteristics (Continued)

Unit	Characteristics
AC Distribution 1A10	Dimensions Height: 7-1/2 inches Width: 19 inches Depth: 5-1/2 inches Finish Primer: Zinc chromate per MIL-P-8585 (ES111-900024) Finish Coat: Enamel, light-gray, semigloss, per TT-E-529, color chip 26314

mounting hole, receiver A2 in the left center position, power control and distribution module A4 in the right center position, and data and ranging module A3 in the extreme right position. They are mounted and secured to the chassis rear panel through mounting holes in flanges around the upper portion of each module housing. Floating hardware is used for mounting the modules to facilitate installation. This method of mounting permits connector receptacles to be positioned outside the RF control unit and facilitates cable connection and removal and replacement of individual modules without disturbing the remaining units and without removing the complete RF control unit from its rack position.

2-6. Data and Ranging Module.

The data and ranging module used in the ISE platform is a modified version of the one data frame configuration used in the IRL Subsystem. Modification to the module permits one to six frames of data to be transmitted by the platform during any particular test. The number of data frames to be used is manually programmed with a six-position rotary switch located on the self-check front panel. Each frame contains 28 switch selected signals which originate at an analog source located in the self-check unit. The analog signals are then switched either to an internal analog source or external source for each of the 28 channels at the analog control panel. Mechanically, the data and ranging module is secured by four mounting screws and comprises an aluminum housing assembly, three internally mounted printed-circuit cards, and three externally mounted connector receptacles. It is 4 inches high, 6 inches wide, 6.5 inches long, and weighs approximately 4 pounds. The aluminum housing consists of separate side, top and bottom, and end plates with flange mounting holes that permit individual pieces to be molded together. Inside the housing, the three printed-circuit cards are evenly distributed and protected by rigid polyurethane foam which is used for potting the electrical components. All external connectors are front mounted to the top panel for easy access. Refer to Table 1 for a detailed tabulation of the physical characteristics.

2-7. Power Control and Distribution Module.

The power control and distribution module housing is also constructed of aluminum and is 2 inches high, 6 inches wide, 6.5 inches long, and weighs approximately 2.9 pounds. Mechanically, it is constructed identically to the data and ranging module. The housing contains two printed-circuit cards and has three front mounted external connector receptacles. This module is secured to the rear panel of the RF control unit with two mounting screws through the mounting flange. In the mounted position, the three connectors are exposed for easy access. Refer to Table 1 for a detailed tabulation' of the module physical characteristics.

2-8. Transmitter/Diplexer Module.

The transmitter/diplexer module is constructed of aluminum and is 4 inches high, 6 inches wide, 6.5 inches long, and weighs 7 pounds. Two crimp type and two coaxial TNC type connectors are mounted on the face of the housing assembly in conjunction with a valve utilized for pressurization. All connectors are easily identified by reference designator markings on the housing. The two crimp type connectors provide data, command, and power

inputs and telemetry point outputs. The TNC connectors provide the antenna input and output to the PCM/FM UHF receiver module. The transmitter module is secured to the RF control unit chassis by four screws through the two mounting flanges. Removal of the top cover plate from the housing assembly exposes the functional circuits that consist of a solid-state driver, power amplifier, diplexer, dc-to-dc converter, pressure transducer, power amplifier temperature transducer, and a solid-state driver thermistor. Refer to Table 1 for the detailed tabulation of physical characteristics.

2-9. Receiver Module.

The receiver module is constructed of aluminum and is 2 inches high, 6 inches wide, 6.5 inches long, and weighs 2.33 pounds. The mechanical housing assembly comprises a maior assembly and three covers that are secured to the top of the maior assembly. Each cover is secured by four phillips-head screws and provides protection to three of the four main functional units. Two crimp type connectors, two TNC type connectors, and one twin axial type connector are secured to the front panel of the housing and are easily identified by reference designator markings. The two crimp type connectors provide input operating voltages and telemetry outputs and the coaxial TNC connectors provide the input from the transmitter/diplexer module and the video output to the data processing circuits in the data and ranging module. The twin axial connector provides a 25 megacycle output for receiver signal-to-noise calibration and use as a relative signal strength indicator. The receiver is mounted to the RF control unit rear chassis plate with two screws through the mounting flanges on the housing assembly. Removal of the three top covers from the maior assembly exposes the functional circuits within. The circuits are segregated into three sections: IF section, RF section, and discriminator and video amplifier section with an internal thermistor. The receiver module also contains a dc-to-dc converter located in the maior assembly.

2-10. IRLS Time Delay Simulator.

The IRLS time delay simulator (1A3) is a customer-supplied unit of equipment designed and constructed for installation in a standard 19-inch equipment rack. The unit is contained in an enclosed chassis 3.5 inches high, 17 inches wide, and 7 inches deep with a 3.5 - by - 19-inch front panel drilled for screw mounting. The unit is mounted with four phillips-head screws through the front panel. Three BNC connectors are mounted on the rear panel and duplicated on the front panel. Once the unit is mounted, either set of connectors may be used. These BNC connectors provide access for the NRZ and 12.5 KC clock inputs and the delayed output signals. In addition, the front panel has an 11-position rotary switch graduated and labelled from 0 to 2000 microseconds with steps 2 through 11 ranging from 1280 to 2000 microseconds in 80-microsecond increments for time delay selection, and a POWER ON/OFF switch and pilot indicator. All controls and switches are easily identified with the appro-. priate designators. In addition to the three connectors, the rear panel contains an &screw connection terminal strip and the AC power cartridge-type fuse mounting.

2-11. Analog Control Panel.

The analog control panel (1A4) is 3.5 inches high, 19 inches wide, and 1.5 inches deep, and it; prepared for a 4-screw mounting in a standard 19-inch equipment rack. The complete assembly, with cable connector mounted, extends 4.5 inches into the rack. The

front panel accommodates 28 sets of 1 toggle switch and 2 test jacks, one combination for each data channel input. The toggle switches are labelled INT (internal) and EXT (external) denoting the external analog source. External analog inputs may be inserted via the respective INPUT test jack, At the rear of the assembly, a 24-inch cable is permanently affixed to the panel stiffeners, and the conductors are terminated at the switches. The other end of the cable is split and terminated into two 61-pin electrical plug connectors. This cable connects the analog control panel switches to the self check assembly and carries the 28 switch selected analog signals to the self-check, and the analog input from the self-contained analog source in the self-check.

2-12. Self-check Unit.

The self-check unit (1A5) is contained in a removable drawer type chassis 9 inches high, 17 inches wide with a 19-inch front panel, and extends 12 inches into the cabinet. The drawer type chassis is slide mounted into the cabinet and secured with eight phillips-head machine screws through the front panel. Handles are provided on the front panel to facilitate removal and transportability. The entire unit is enclosed with top and bottom covers secured to the chassis side panels with machine screws. With the self-check unit removed from its rack position, the top cover plate can be removed, thus exposing the functional components within the drawer. The functional components comprise the self-check logic, attenuator AT1, and oscillator assembly Y2 mounted in a fabricated card tray located through the center of the drawer. Two additional attenuators, AT2 and AT3, are mounted on the rear panel and a plug-in relay assembly (K1) is located on the inside left panel in a tube socket mounted on the panel. A retainer bracket is bolted to the relay mounting bracket and must be removed prior to replacing the relay. The maior self-check functional circuits are contained on plug-in printed-circuit logic cards A1 through A10 and are exposed for replacement after removing the top cover plate of the drawer. The circuits on these cards are power supply A1, lamp drivers and analog source A2, S-meter and event recorder amplifier A3, range pattern logic A4, address register A5, error detector A6, and address and data correlator A7 through A10. The self-check front panel accommodates the necessary switches and indicators for self-check programming and monitoring. Programming is accomplished with 16 toggle switches located in the upper left-hand corner of the panel. These switches are used to select the 16-bit address code and each is appropriately labelled in binary notation. Three rotary switches, also used for programming, are located adjacent to the ADDRESS switches. The three switches are located veritcally on the right center of the panel and comprise the 3-position MODE, 6-position FRAME, and 3-position ANALOG SCALE switches. For monitoring purposes, a panel of 32 test points is located directly below the ADDRESS switches and a STATUS grouping is located on the extreme right hand side of the front panel. The STATUS grouping comprises the GO/NO GO indicators and a manual RESET pushbutton. The lower right-hand corner of the panel contains the POWER ON/OFF switch. The rear of the self-check chassis contains all the input/output connectors, J101 through J110, to and from the unit. Connectors J101 through J107 are N-type connectors, except J104. which provide interconnection between the RF control unit and the self-check. J104 is a MICRODOT type connector which provides the power input to the internal logic circuits. Connectors J108 and J109 accept the twin 61-pin plug connectars from the analog control panel cable assembly. Connector J110 is a 19-pin connector attached to the S-meter and event recorder logic providing the inputs and outputs between the self-check and RF control unit.

2-13. RF Control Unit.

The RF control unit (1A6) is contained in a drawer type chassis 10.5 inches high, 17 inclres wide with a 19-inch wide front panel, and extends 19.5 inches into the cabinet, The drawer type chassis is slide mounted on angle brackets within the system cabinet and secured with eight Phillips-head machine screws through the front panel. The RF control assembly contains the IRLS platform which is inserted through an aperture 6 inches high and 12 inches wide in the rear panel and secured to floating hardware welded to the panel. The platform is thus accessabie from the rear of the system without removal of the RF control unit. All platform connectors and one 19-pin connector (J3) are located at the rear of the unit. No connections to the platform are made within the drawer. Connector J3 provides an outlet for the signal leads between the S-meter on the drawer panel and the S-meter and event recorder logic in the self-check unit. Components within the drawer are accessible through the top of the unit once the drawer is withdrawn from the cabinet. These components are the IRLS platform modules, the 15DB attenuator AT2 located in the center, the directional coupler mounted on the right side wall, and the backs of all panel-mounted switches, connectors, and meter. The front panel provides a mounting area for three rotary switches, a vernier control, the S-meter, and two type N connectors. Of the three rotary switches, one is located in the upper left hand section of the front panel. This is a 2-position rotary switch for a coarse attenuation selection of 0 DB and 30 DB and is associated with a VERNIER ATTENUATION control mounted directly below it. The VERNIER ATTENUATION control (AT1) is a turret attenuator with a range from 0 DB to 109 DB. The second rotary switch is a 3-position RANGE select switch associated with the S-meter on the upper center of the panel. The RANGE switch is capable of selecting a LOW, MID, or HIGH range scale. The third rotary switch is the 2-position RF MODE select switch, and it is located in the upper right hand section of the front panel. Operation of this switch selects either PLATFORM or SELF-CHECK operating modes. Located directly below the RF MODE switch are two type N connectors for DIRECTIONAL COUPLER OUTPUTS. One connector, RF POWER, is connected to the output of the 20 DB attenuator AT3, and the other, COUNTER, is the output connector for the directional coupler DC1 within the unit drawer.

2-14. AC Distribution Panel.

The AC distribution panel (1A10) is an enclosed panel-mounted chassis 7.5 inches high, 17 inches wide, and 5.5 inches deep mounted on a 19-inch wide front panel. Access to the panel assembly is gained through the rear cabinet door. The panel is located directly opposite meter rack adapter 1A2 and secured to the equipment rack with four phillips-head machine screws. The front panel provides a mounting surface for a circuit-breaker type ON/OFF switch, an elapsed-time meter, and a power relay located within the chassis. Removal of the top plate exposes the internal switch and meter connections and the panel-mounted power relay. Three box connectors are mounted on the rear panel for all AC input and output wiring.

2-15. ELECTRICAL CHARACTERISTICS.

Table 2 provides a listing and summation of the electrical characteristics and operating parameters of each drawer and/or modular unit comprising the ISE and overall signal information pertaining to the IRL Subsystem. For additional information concerning Electronic

Table 2. Electrical Characteristics and Operating Parameters.

Unit	Function	Characteristic/Parameter
Subsystem Signals	Minor Bit	80 microseconds.
	Bit Rate	12.5 KC.
	Range Word	12 minor bits.
	Range Word Duration	960 microseconds.
	Range Word Rate	1.041 KC.
	M-Word	First 8 minor bits of range word.
	N-Word	Last 4 minor bits of range word.
	Major Bit	One 12 minor bit range word.
	Major Bit Value	Represented by M-Word.
	Binary ONE	10101100
	Binary ZERO	31010011
	Sync Words	Represented by N-Word.
	Pattern Xync	Bit Value: 0110
	Word Sync	Bit Value: 1001
	Platform Address	16 range Words.
	Data Word	7 Range Words.
	Data Word Value	
	Binary ONE	10101100
	Binary ZERO	31010011
	Data Frame	Three 16 range word platform addresses; 28 data words.
	Power Requirement	
	Standby	14.21 watts,
	Operate	127.63 watts.
Equipment Rack	Input	110 vac ± 10 percent, 60 cps @ 10 amperes.
Electronic Counter 1A1 (517532-G1 Configuration Only)	Input	
	Voltage	110 vac ± 10 percent.
	Sensitivity	100 millivolt rms, minimum.
	Coupling	AC or DC with separate BNC connectors.
	Attenuation	0.1, 1, or 10 volts.

Table 2. Electrical Characteristics and Operating Parameters.

Unit	Function	Characteristic/Parameter
Electronic Counter 1A1 (517532-G1 Configuration Only) (Continued)	Registration	Eight digits in-line with digital indicator tubes. Maximum storage display of *99,999,999* which is less than seven inches wide.
	Sample Rate	Time between measurement cycles is continuously variable from 0.1 second to 5.0 seconds. A display of a single measurement can be held indefinitely.
	Impedance	One megohm is parallel with approximately 25 pf.
	Allowable Overload	120 volts rms on 0.1 volt range. 250 volts rms on 1 volt range. 500 volts rms on 10 volt range.
	AC Coupling Capacitance	0.022 µf at 600 volts.
	Remote Operation	Rear-panel connectors permit complete remote control of all front panel control functions (except sample rate and sensitivity) by contact closure or electronic switching. Source of -15 volts for gate control circuits and +170 volts for decimal point and measurement unit control circuits is provided.
	Frequency Measurements	
	Range	0 to 50 megacycles.
	Gate Time	1 microsecond to 10 seconds in decade steps.
	Accuracy	± 1 count ± time base accuracy.
	Reads In	Kilocycles or megacycles with positioned decimal point.
	Self Check	Counts 10 megacycles at gate time selected on time base switch.

Table 2. Electrical Characteristics and Operating Parameters (Continued).

Unit	Function	Characteristic/Parameter
Electronic Counter 1A1 (continued)	Period Average Measurements Range	
	Single Period	0 to 1 megacycle.
	Multiple Period	0 to 300 kilocycles.
	Periods Averaged	1, 10, 10^2, 10^3, 10^4, 10^5.
	Accuracy	± 1 count ± time base accuracy ±(trigger error periods averaged). Trigger error is 0.3 percent for sinewave with 40 db signal-to-noise ratio.
	Frequency Counted	
	Single Period	10 megacycles to 1 cps in decade steps.
	Multiple Period	10 megacycles to (number of periods averaged - 10) cps in decadesteps.
	Reads In	Seconds, miliiseconds, and microseconds with positioned decimal point and displays measurement unit.
	Self Check	Gate time is 10 microseconds to 1 second (periods averaged of 100 kilocycles). Counts at a 100 kilocycle rate.
	Ratio Measurements Displays	(f_1/f_2) times psriod multiplier which is 1 to 10^5 in decade steps.
	Range	
	f_1	0 to 50 megacycles.
	f2	0 to 1 megacycle in single period. 0 to 300 kilocycles in multiple periods with 10 to 10^5 periods averaged in decade steps.

Table 2. Electrical Characteristics and Operating Parameten (Continued).

Unit	Function	Characteristic/Parameter
Electronic Counter 1A1 (Continued)	Accuracy	± 1 count of f_1 ± (trigger error of f_2; number of periods averaged), Positioned decimal point for number of periods averaged.
	Scaling Frequency Range Factor	3 to 50 megacycles. $10 - 10^9$ in decade steps.
	Internal Time Base Frequency	1 megacycle.
	Aging Rate After 75 Hours	Less than $\pm 2 \times 10^{-8}$ per week or less than $\pm 3 \times 10^{-9}$ per day.
	Temperature Stability	Less than $\pm 2 \times 10^{-10}$ per °C.
	Line Voltage Stability	Less than $\pm 5 \times 10^{-10}$ for 10 percent change in line voltage from 115 vac.
	Short Term Stability	Less than $\pm 5 \times 10^{-10}$ (1-second averaging time) with constant temperature and line voltage.
	Adjustments	Fine control for range of approximately 4×10^{-8} and medium frequency control for a range of approximately 1×10^{-6} are availabie from the front through the plug-in compartment. Coarse frequency control for a range of 1×10^{-5} is available at the rear.
	Output Frequencies Rear Panel	0.1 cps to 10 megacycles selectable in decade steps.
	Front Panel	0.1 cps (1v p-p) to 1 megacycle selectable in decade steps.

Table 2. Electrical Characteristics and Operating Parameters (Continued).

Unit	Function	Characteristic/Parameter
Electronic Counter 1A1 (Continued)	External Time Base	1 megacycle (1v rms into 1000 ohms) input at rear panel.
	Frequency Converter	
	Range	50 megacycles to 500 megacycles using mixing frequencies of 100 megacycles to 500 megacycles in decade steps.
	Input Voltage	50 millivolts rms to 1 volt rms (-13 dbm to +13 dbm).
	Overload	2 volts rms.
	input Impedance	Approximately 50 ohms.
	Level Indicator	Acceptable voltage level indication,
	Registration	Counter display is added to or subtracted from converter dial reading depending on whether the mixing frequency is below or above the measured frequency.
Electronic Voltmeter 1A2	Input Voltage	115/230 vac ± 10 percent.
	Power	13 watts (20 watts with 11036A ac probe).
	Frequency	50 to 1000 cps.
	DC Voltmeter	
	Voltage Ranges	± 15 millivolts to ± 1500 volts full scale in 11 ranges.
	Accuracy	± 2 percent of full scale in any range.
	Input Resistance	100 megohms ± 1 percent in 500 millivolt and above and 10 megohms ± 3 percent on the 15, 50, and 150 millivolt ranges.

Table 2. Electrical Characteristics and Operating Parameters (Continued).

Unit	Function	Characteristic/Parameter
Electronic Voltmeter 1A2 (Continued)	DC Ammeter	
	Current Ranges	± 1.5 microampere to 150 milliamperes full scale in 11 ranges.
	Accuracy	± 3 percent of full scale in any range.
	Input Resistance	Decreasing from 9 K ohms in 1.5 microampere range to approximately 0.3 ohm in the 150 milliampere range.
	Ohmmeter	
	Resistance Range	10 ohms to 10 megohms (center scale) in 7 ranges.
	Accuracy	Zero-to-midscale: ± 5 percent of reading or ± 2 percent of midscale, whichever is greater. ± 7 percent from midscale to scale value of 2. ± 8 percent from scale value between 2 to 3. ± 9 percent between scale values 3 to 5. * 10 percent between scale values 5 to 10.
	Amplifier	
	Voltage Gain	100 maximum.
	AC Rejection	3 db at 0.5 cps. Approximately 66 db at 50 cps and higher frequencies for signals less than 1600 volts peak or 30 times full scale, whichever is smaller.
	Isolation	Impedance between common and chassis is greater than 10 megohms in parallel with 0.1 microfarad.

Table 2. Electrical Characteristics and Operating Parameters (Continued).

Unit	Function	Characteristic/Parameter
Electronic Voltmeter 1A2 (Continued)		Common may be floated up to 400 vdc above the chassis for dc and resistance measurements.
	output	Proportional to meter indication. 1.5 vdc at full scale. Maximum current is 1 milliampere.
	Output Impedance	Less than 3 ohms at dc.
	Noise	Less than 0.5 percent of full scale in any range (p-p).
	DC Drift	Less than 0.5 percent of full scale/ year at constant temperature. Less than 0.02 percent full scale/ °C.
	Overload Recovery	Recover from a 100 to 1 overload in less than 3 seconds.
	AC Voltmeter	
	Voltage Ranges	0.5 volt full scale to 300 volts in a 0.5, 1.5, 5 sequence in 7 ranges,
	Accuracy	± 3 percent of full scale at 400 cps. for sinusoidal from 0.5 to 300 volts rms.
	Frequency Respons	± 2 percent from 100 cps to 100 megacycles (400 cps reference). ± 10 percent from 20 cps to 100 cps and from 100 megacycles to 700 megacycles.
	Frequency Range	20 cps to 700 megacycles.
	Input Impedance	Input capacity of 1.5 picofarad. Input resistance is greater than 10 megohms at low frequencies

Table 2. Electrical Characteristics and Operating Parameter (Continued).

Unit	Function	Characteristic/Parameter
Electronic Voltmeter 1A2 (Continued)		and drops off at high frequencies due to dielectric loss.
	Meter	Individually calibrated taut-band meter responds to positive peak-above-average and is calibrated in rms volts for sinewave input.
	Maximum Input	DC: 100 vdc on 15, 50, and 150 millivolt ranges. 500 vdc on 0.5 to 15 volt ranges and 1600 vdc on higher ranges. AC: 100 times full scale or 400 volts peak, whichever is less.
Power Meter 1A2	Input Voltage	115/230 vac ± 10 percent.
	Frequency	50 to 400 cps.
	Power	2-1/2 watts.
	Power Ranges	Seven ranges with full-scale readings of 10, 30, 100, and 300 microwatts and 1, 3, and 10 milliwatts. Also calibrated from -20 dbm to +10 dbm full scale in seven 5 db steps.
	Accuracy	At +20°C to +35°C, ± 1 percent of full scale in 100 microwatt range and above, ± 1.5 percent of full scale in 30 microwatt range, and ± 2 percent of full scale in 10 microwatt range. At 0°C to +55°C, ± 3 percent in all ranges.

Table 2. Electrical Characteristics and Operating Parameters (Continued).

Unit	Function	Characteristic/Parameter
Power Meter 1A2 (Continued)	Calibration Factor	Normalizes meter reading to account for thermistor mount calibration between 88 and 100 percent in 1 percent steps.
	Meter	Individually calibrated mirror-backed scale with taut-band suspension,
	Zero Carryover	Less than 1 percent of full scale when zeroed on most sensitive range.
	Zero Balance	Continuous control about zero point. Range below zero is equivalent to at least 3 percent of full scale.
	Voltmeter Output	With minimum load impedance of 500 K ohms, output is 1 vdc ± 3 percent at full scale meter deflection.
	Recorder/Leveler output	With minimum load impedance of 600 ohms, output is approximately 1 vdc at full scale meter deflection.
IRLS Time Delay Simulator 1A3	Inputs	
	Primary Voltage	115 vac ± 10 percent.
	Frequency	50 cps ± 10 percent.
	Logic Levels	
	Binary ONE	2.5 ± 0.5 vdc.
	Binary ZERO	3.0 ± 0.3 vdc.
	Data Format	NRZ-Up level is logic ONE.
	NRZ Bit Rate	12.5 KB.
	Clock	12.5 KC.

Table 2. Electrical Characteristics and Operating Parameters (Continued).

Unit	Function	Characteristic/Parameter
IRLS Time Delay Simulator 1A3 (Continued)	output	NRZ: Either not delayed or delayed between 1280 and 2000 microseconds in 80 microsecond increments.
Analog Control 1A4	Inputs/Outputs	Simulated analog transducer.
	Quantity	28: One per data word.
	Level	Zero-scale: 0 vdc. Half-scale: -3.225 vdc. Full-scale: -6.4 vdc.
Self Check 1A5	Logic Levels Binary ONE Binary ZERO	 4.5 ± 1.0 vdc. 0.0 ± 0.3 vdc.
	Input Frequency	466.00 megacycles.
	input Frequency Attenuation	55 dbm.
	Local Oscillator Frequency	64.5 MC.
	Mixer Output Frequency	401.5 megacycles.
	Mixer Output Attenuation	40 db.
	Platform Mode Output Attenuation	15 db minimum.
	Receiver IF Input	25 megacycles.
	Modulated Digital Subcarrier	12.5 KC range word sequence that modulates the transmitter.
	Simulated Analog Transducer Output	28: One per data word.
	Level	Zero-scale: 0 vdc. Half-scale: -3.225 vdc. Full-scale: -6.4 vdc.
	Logic Clock	25 KC.

Table 2. Electrical Characteristics and Operating Parameters (Continued).

Unit	Function	Characteristic/Parameter
RF Control 1A6	Power Meter Output Attenuation	Fixed 39.2 db.
	Self Check Mode Attenuation	Fixed 30 db.
	Normal Mode Attenuation	Hardwired 30 db.
	Attenuation Range	Variable: 30 through 139 db.
Transmitter/Diplexer 1A6A1	Inputs DC Power Input	-24.5 ±1 vdc at 5.2 amps maximum. 4.5 amps nominal.
	Standby Mode Power Input	-24.5vdc at 10 watts.
	Ripple	65 millivolts peak-to-peak between 100 cps to 14 KC superimposed on dc supply voltage.
	Transient Inputs	Survive 0 to -33v for up to 5 milliseconds.
	Warmup Time	120 seconds.
	Base Voltage Regulation	±2 percent.
	Duty Cycle	10 minutes on; 80 minutes off.
	Crystal Frequency	58.25 megacycles ±0.0015 percent,
	Modulation Type	PCM/FM.
	NRZ PCM Bit Rate	112.5 KC.
	Sensitivity	1KC/volt at 50 megacycle point; 8 KC/volt at 466 megacycle point.

Table 2. Electrical Characteristics and Operating Parameters (Continued).

Unit	Function	Characteristic/Parameter
Transmitter/Diplexer 1A6 A1 (Continued)	Peak Frequency Deviation	±30 KC at 400 megacycles.
	Frequency Response	dc to 50 KC + 0, -3 db.
	Impedance	20,000 ohms ±10 percent.
	Level	3.0 volts peak far 24 KC peak deviation.
	Linearity	±5% at 20 KC peak deviation.
	outputs	
	Frequency	466.0 megacycles,
	Power Output	25 watts nominal at diplexer output.
	Frequency Stability	±0.0015 percent.
	Amplitude Modulation	Less than 5 percent.
	Power Requirements	
	Standby	10.0 watts.
	Operate	122.0 watts,
	Operational Check	
	Warmup Time	120 seconds.
	Telemetry Monitor Points	
	Power Amplifier Temperature Sensing	0 to -6.4 vdc.
	Solid State Driver Temperature Sensing	0 to -6.4 vdc,
	Power Amplifier Plate Current	0 to 6.4 vdc.

Table 2. Electrical Characteristics and Operating Parameters (Continued).

Unit	Function	Characteristic/Parameter
Transmitter/Diplexer 1A6 A1 (Continued)	Transmitter ON Command	0 to -6.4 vdc.
	Transmitter OFF Command	0 to -6.4 vdc.
	Source Impedance	5,000 ohms maximum except temperature sensors which have 6,7000 ohms maximum.
Diplexer	Transmitter-to-Receiver Isolation	85 db minimum.
	Receiver-to-Transmitter Isolation	20 db.
	Transmitter Filter insertion Loss at 466.0 mc	0.4 db.
	Insertion Loss at 401.5 ±50 mc	Greater than 30 db.
	Receiver Filter	
	Insertion Loss at 401.5 mc	1.2 db.
	Insertion Loss at 466.0 mc	Greater than 65 db,
	Impedance	50 ohms.
Receiver 1A6 A2	Inputs DC Power Input	-24.5 fl vdc at 80 ma. maximum. 60 ma. nominal.
	Input Frequency	401.5 megacycles.
	Frequency Response	±0.001 percent,

Table 2. Electrical Characteristics and Operating Parameters (Continued).

Unit	Function	Characteristic/Parameter
Receiver 1A6 A2 (Continued)	Noise Figure	4 db maximum at input terminal.
	Dynamic Range	80 db minimum.
	Impedance	50 ohms nominal.
	Bandpass Ripple	±0.5 db.
	Spurious Response (with diplexer)	Image rejection 60 db minimum; all other frequencies are 8 db minimum.
	Base Voltage Regulation	±2 percent.
	Ripple	55 millivolts peak-to-peak between 100 cps to 14 KC superimposed on dc supply voltage.
	Transient Inputs	Survive 0 to -33v for up to 5 milliseconds.
	outputs Video	1v peak-to-peak * 10% for 20 KC peak deviation.
	25 mc IF	Utilized for noise figure calibration.
	Video Response	5 cps, +0, -3db, to 50 KC, +0, -1db.
	Output Impedance	100 ohms.
	Time Delay	±0.50 microseconds for ±20 KC.
	Duty Cycle	Continuous.
	Format	NRZ
	Power Requirement	.96 watts.

Table 2. Electrical Characteristics and Operating Parameters (Continued).

Unit	Function	Characteristic/Parameter
Receiver 1A6A2 (Continued)	Telemetry Monitor Point Receiver Module Temperature Sensing	0 to -6.4 vdc.
	Sensor Impedance	6,700 ohms.
Data and Ranging 1A6 A3	Logic Levels	
	Binary ONE	2.5 ±0.5 vdc.
	Binary ZERO	0.0 ±0.3 vdc.
	Input Requirement Receiver A2	
	Level	4.8v ±20 percent.
	Format	NRZ-Up level is logic ONE.
	Load	220 ohms ±10 percent.
	Transducer Analog Data	28.
	Level	0 to -6.4 vdc unloaded.
	Source Impedance	Less than 20,000 ohms.
	Dynamic Response	Sampling error of less than 1% at rate of input voltage change of 10^4 volts/sec.
	Power Control and Distribution Operating Voltages	Regulated -24.5 ±1 vdc. ±15 vdc. ± 9 vdc. + 6 vdc. + 3.4 vdc.
	Outputs	
	Modulated Digital	12.5 KC modulated logic level output to modulator driver.

Table 2. Electrical Characteristics and Operating Parameters (Continued).

Unit	Function	Characteristic/Parameter
Data and Ranging 1A6 A3 (Continued)	Operating Logic Levels	Binary ONE: 2.5 ±0.5 vdc. Binary ZERO: 0.0 ±0.3 vdc.
	Test Points	
	Format Word Shift	Clock pulse output from Platform Logic that is at a logic ONE level at the beginning of each new data word and utilized in the formatter column counter.
	$\overline{\text{Data}}$ Gate	Logic ONE level during the time encoded data words are inserted into Address Register and Digital Multiplexer.
	Regenerated 12.5 KC Clock	A 50% duty cycle squarewave with an 80 microsecond period.
	BCE Regenerated 1 KB Data	Data word stream output to Bench Checkout Equipment whose level describes the binary value of the data word.
	Modulated Digital Subcarrier	12.5 KC range word sequence that modulates the Transmitter.
	Error Threshold	Logic ONE level when synchronization is achieved between PCM Demodulator and Bit Synchronizer and Receiver Output,
	Format Flip-Flop	Arrives at Logic ONE level prior to generation of first data frame. Remains at Logic ONE during frame generation and returns to Logic ZERO at transmitter turn-off.

Table 2. Electrical Characteristics and Operating Parameters (Continued),

Unit	Function	Characteristic/Parameter
Data and Ranging 1A6A3 (Continued)	Regenerated 1 KC Clock	Logic ONE level during N-word portion of 1 KC range word data bit.
	Telemetry Holdoff	Logic ZERO level coincident with platform address recognition until end-of-frame or end-of-three seconds.
	Telemetry Monitor Points	Sensing devices that monitor temperature and voltage conditions to generate analog voltages.
	VCO Error Voltage	0 to -6.4 vdc.
	VCC Voltage	0 to -6.4 vdc.
	Logic Temperature	0 to -6.4 vdc.
	Sensor Impedance	Voltage 5,000 ohms. Temperature 6,700 ohms.
	Power Requirement	1.421 watts.
Power Control and Distribution 1A6A4	Logic Levels Binary ONE Binary ZERO	 2.5 ±0.5 vdc. 0.0 ±0.3 vdc.
	Inputs	Operating logic levels. Modulated digital subcarrier. -24.5 ±1 vdc.
	Outputs Transmitter ON	 + 24 vdc pulse coincident with address sync.
	Transmitter OFF	+ 24 vdc pulse coincident with end-of-frame or end-of-three seconds.
	Data Modulation	Regulated logic level output from platform equipment utilized to modulate the transmitter.

Table 2. Electrical Characteristics and Operating Parameters (Continued).

Unit	Function	Characteristic/Parameter
Power Control and Distribution 1A6 A4 (Continued)	Signal Level	30 ±0.2v peak when loaded with 20K ohms to ground.
	Source Impedance	Less than 1,000 ohms.
	Rise and Fall Times	72 ±1.0 microseconds.
	Overshoot and Ripple	Less than 0.3v.
	Operating Voltages	Regulated -24.5 ±1 vdc.
	Regulation	±2 percent.
	Ripple	55 millivolts peak-to-peak between 100 cps and 14 KC superimposed on dc supply voltage.
	Transient Inputs	) to -33 vdc for 5.0 milliseconds.
	Output Impedance	Less than 0.12 ohm,
	Power Requirement	1.83 watt.
	Telemetry Monitor Points	
	Preregulator Temperature	) to -6.4 vdc.
	Preregulator Voltage	) to -6.4 vdc.
	-24.5 vdc Input	) to -6.4 vdc.
Event Recorder 1A7	Input Voltage	03 to 127 vac.
	Frequency	50 to 400 cps.
	Power	50 watts, maximum.

Table 2 Electrical Characteristics and Operating Parameters (Continued).

Unit	Function	Characteristic/Parameter
Event Recorder 1A7 (Continued)	Time Resolution	Can respond to events as brief as 1.3 milliseconds with all writing controls at maximum speed.
	Time Duration Accuracy	Combined error, chart drive and paper, does not exceed 1 percent. All others combined are ± 0.5 millimeters.
	Simultaneous Events	Less than 0.25 millimeter error with a 1.25 millimeter maximum error between any two channels,
	Chart Speeds	1, 5, 20, and 100 mm/sec.
	Logic Levels Binary ONE Binary ZERO	 3.5 ±1.0 vdc. 0.0 ±0.3 vdc.
	Write Level	Logic ONE.
	Inputs	Receipt of Address: Indicated by transition of the Telemetry Hold-off signal from logic ZERO to logic ONE coincident with platform address recognition, Acquisition of Phase Lock: Indicated by transition of the Error Threshold signal from logic ZERO to logic ONE when synchronization is achieved between the PCM Demodulator and Bit Synchronizer and Receiver output. Receipt of Address Complement: Indicated by transition of the Format Flip-Flop signal from logic ZERO to logic ONE coincident with platform address complement recognition.

Table 2. Electrical Characteristics and Operating Parameters (Continued)

Unit	Function	Characteristic/Parameter
Event Recorder 1A7 (Continued)		Total Satellite Transmission Time: Indicated by detecting the IF output from the platform receiver,,
Power Supply 1A8	Input Voltage	105 to 125 vac, single phase.
	Frequency	50 to 400 cps.
	Response Time	25 microseconds.
	Output Voltage	18 to 36 vdc.
	Output Current	0 to 8 amperes (maximum).
	Regulation	±0.01 percent.
	Output Impedance	250 microhenries + 0.3 microhenries.
Centrifugal Fan 1A9	Input Voltage	115 vac *10 percent.
	Power Amperes Watts	 1 90
	Motor Speed	3000 rpm.
	Air Discharge Direction	Rearward.
	Air Volume	300 cubic feet/minute.

counter 1A1, power meter and electronic voltmeter 1A2, IRLS time delay simulator 1A4, event tecorder 1A7, and power supply 1A8, refer to the appropriate vendor instruction manual.

2-16. APPLICABLE DOCUMENTS.

individual documents containing information revelant to the work accomplished during the performance of this contract includes the Volume I Integration Support Equipment Instruction Manual, the Volume II Self-check Tester Instruction Manual, the Final Report for the Interrogation, Recording, and Location Subsystem, dated June 1967, and the Volume I Platform Electronics and Telemetry Equipment Instruction Manual.

SECTION III

FUNCTIONAL THEORY OF OPERATION

3-0. FUNCTIONAL THEORY OF OPERATION.

3-1. SCOPE.

This section of the report provides information necessary for the understanding of the functional operation of the Integration Support Equipment in conjunction with the platform operation. The discussions pertaining to the functional operation progress through each operational mode of the ISE and an overall analysis of platform operation.

3-2. ISE FUNCTIONAL DISCUSSION.

3-3. General.

The function of the Integration Support Equipment is to provide a method of verifying correct operation and operating parameters of the IRLS satellite during integration into the Nimbus Spacecraft, immediately prior to launch, and during post launch operation. The ISE is also capable of performing a self-check operation to verify the internal platform's ability to accurately process data, thus ensuring successful communication between the ISE and the Nimbus-borne IRLS satellite. Removing the self check drawer from the equipment rack enables personnel to perform self-check operations on platforms external to the ISE. These functions are made possible by switch programming the ISE to function in three distinct operational modes. All three modes are programmed from the self check and RF control panels. The directly cabled or close proximity mode allows IRLS satellite checkout during Nimbus integration or immediately prior to launch after the Nimbus Spacecraft has been installed into the launch vehicle. The normal platform mode permits IRLS satellite checkout in any orbital pass during the mission (if the ISE platform address code is programmed into the satellite command memory). The self-check mode may be initiated at any time it is necessary to verify ISE platform operation or operation of a platform external to the ISE.

During the directly cabled, close proximity, or normal platform mode, the IRLS satellite must be preprogrammed by the Ground Acquisition and Command Station (GA&CS) to initiate ISE platform interrogation. interrogation is initiated by a continuous transmission of the applicable platform address code at a predetermined time. During an interrogation, the ISE functions as a signal path for the satellite and platform inputs and outputs and also provides zero scale (0 vdc), half scale (-3.225 vdc), or full scale (-6.4 vdc) simulated analog transducer voltages for encoding in the data and ranging module. Correct or improper operation of the satellite and platform may be determined by observing the traces on the event recorder.

During the self-check mode, the ISE is capable of checking and verifying operation of platforms that have all 28 data channels available or platforms that have six hardwired data channels and 22 available data channels. The contents of each data line (two data channels) in each data frame is checked by a unique data verifier in the data correlators that examines the zero-scale, halfscale, and full-scale analog input codes. These data line codes differ by only four 1 KC bits and are examined in the following form.

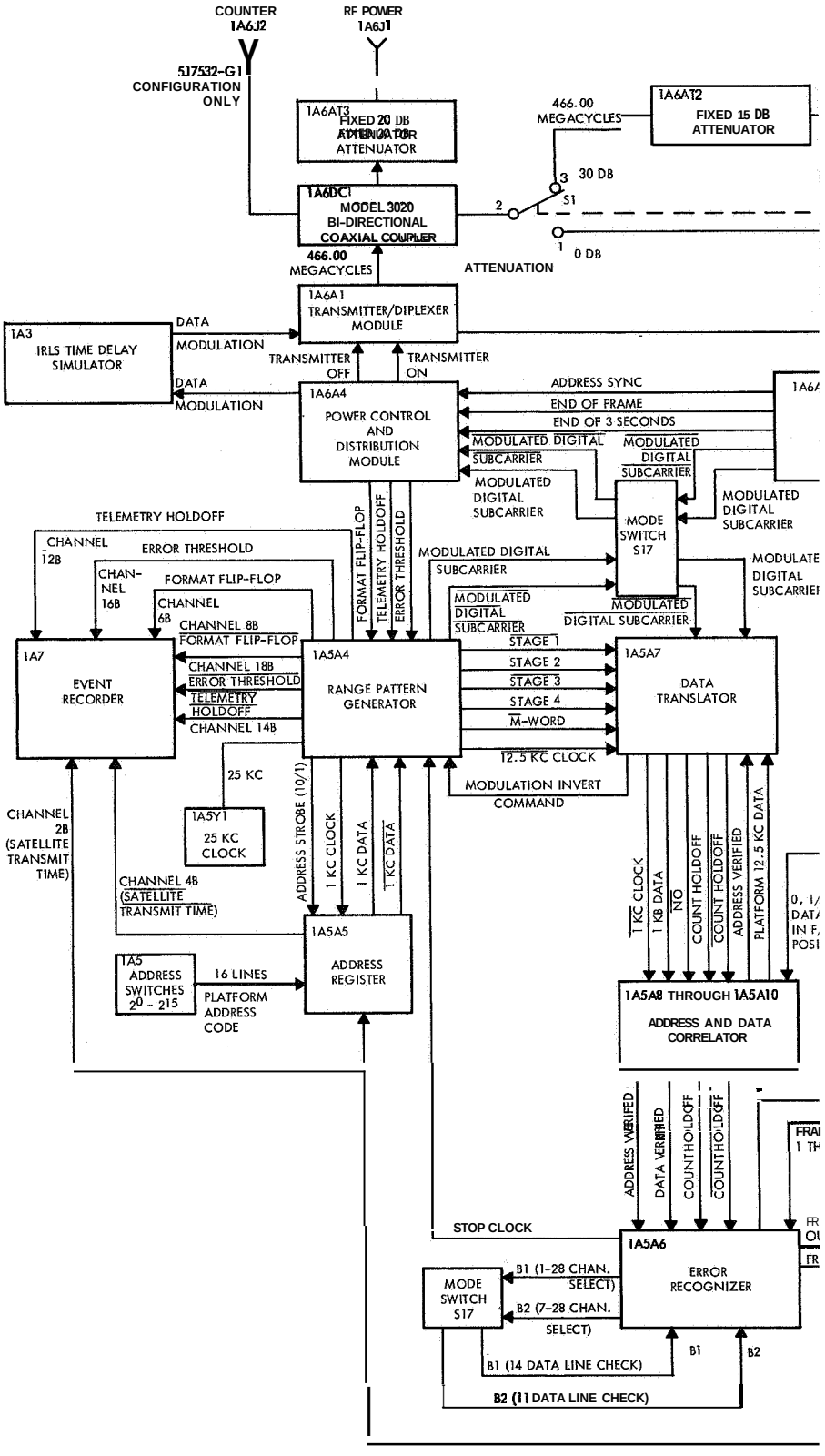
Data Line Containing	Bit 16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Two zero-scale codes (inverted)	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
Two halfscale codes (inverted)	0	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1
Two full-scale codes	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

Note that the data for the zero scale and half scale codes are inverted and that the full scale code is not. The inversion is due to generation of a MODULATION INVERT COMMAND upon recognition of a correct platform address code. This command instructs both the range pattern generator and the data translator to invert the data. An inhibit is placed on the data translator during full scale operation. Noninversion of the full-scale code is required because the coder outputs during full-scale voltage inputs have a data value of logic ONE. As shown above, only bit positions 7, 8, 15, and 16 are examined to identify the individual data channel (word) which, in turn, identifies frame data lines. Counters in the error recognizer verify that the correct number of address complements (3) and data lines (14 or 11) are present in the data frame format.

The block diagram for the Integration Support Equipment is illustrated in Figure 11. The ISE comprises slide-mounted vendor or GFE equipment drawers, a drawer containing rf fixtures and the platform modules, and a drawer containing the logic for self-check. These drawers include electronic counter 1A1 (517532-G1 configuration only), RF power meter and electronic voltmeter 1A2, IRLS time delay simulator 1A3, analog control 1A4, self-check 1A5, RF control 1A6, event recorder 1A7, and blower 1A9. The following paragraphs provide a block diagram discussion of the ISE as it functions in its various operational modes.

3-4. Self-Check Mode.

Operation in the self-check mode is initiated by placing RF MODE switch S2 to the SELF CHECK position, INITIAL ATTENUATION switch S1 to the 30 DB position, VERNIER ATTENUATION control AT1 to the 0 db position, selecting the correct platform address code on self-check ADDRESS switches 2^0 through 2^{15} to correspond to the hardwired address code in data and ranging 1A6A3, placing MODE switch S17 to the 1-28 or 7-28 position, and depressing the RESET pushbutton on self-check 1A5. Depressing the RESET pushbutton generates a FALSE ADDRESS SYNC pulse that is routed to power control and distribution 1A6A4 to generate the TRANSMITTER ON command. This command activates transmitter/diplexer 1A6A1 for data transmission. In this mode, address register 1A5A5 generates a 16-bit platform address code as determined by the positions of ADDRESS switches 2^0 through 2^{15}. The address code is shifted through the address register by the 1 KC CLOCK pulses and the resultant 1 KC DATA and 1 KC $\overline{\text{DATA}}$ outputs are provided to range pattern generator 1A5A4. The input data is modulated by 12.5 KC M-words and N-words that are developed in range pattern generator 1A5A4 to produce the MODULATED DIGITAL SUBCARRIER and $\overline{\text{MODULATED DIGITAL SUBCARRIER}}$ outputs to MODE switch S17. in the 1-28 or 7-28 positions, this switch routes the


COUNTER
1A6J2
RF POWER
1A6J1
5J7532-G1
CONFIGURATION
ONLY
1A6AT3
FIXED 20 DB
ATTENUATOR
466.00
MEGACYCLES
1A6AT2
FIXED 15 DB
ATTENUATOR
3
30 DB
S1
2
1
0 DB
ATTENUATION
1A6DC1
MODEL 3020
BI-DIRECTIONAL
COAXIAL COUPLER
466.00
MEGACYCLES
1A6A1
TRANSMITTER/DIPLEXER
MODULE
1A3
IRLS TIME DELAY
SIMULATOR
DATA
MODULATION
TRANSMITTER
OFF
TRANSMITTER
ON
DATA
MODULATION
1A6A4
POWER CONTROL
AND
DISTRIBUTION
MODULE
ADDRESS SYNC
END OF FRAME
END OF 3 SECONDS
MODULATED DIGITAL
SUBCARRIER
MODULATED
DIGITAL
SUBCARRIER
MODULATED
DIGITAL
SUBCARRIER
MODULATED
DIGITAL
SUBCARRIER
MODE
SWITCH
S17
MODULATED
DIGITAL
SUBCARRIER
TELEMETRY HOLDOFF
CHANNEL
12B
ERROR THRESHOLD
CHAN-
NEL
16B
FORMAT FLIP-FLOP
CHANNEL
6B
CHANNEL 8B
FORMAT FLIP-FLOP
FORMAT FLIP-FLOP
TELEMETRY HOLDOFF
ERROR THRESHOLD
MODULATED DIGITAL
SUBCARRIER
MODULATED
DIGITAL
SUBCARRIER
MODULATED
DIGITAL SUBCARRIER
MODULATE
DIGITAL
SUBCARRIE
1A7
EVENT
RECORDER
CHANNEL 18B
ERROR THRESHOLD
TELEMETRY
HOLDOFF
CHANNEL 14B
1A5A4
RANGE PATTERN
GENERATOR
STAGE 1
STAGE 2
STAGE 3
STAGE 4
M-WORD
12.5 KC CLOCK
MODULATION INVERT
COMMAND
1A5A7
DATA
TRANSLATOR
25 KC
1A5Y1
25 KC
CLOCK
CHANNEL
2B
(SATELLITE
TRANSMIT
TIME)
CHANNEL 4B
(SATELLITE
TRANSMIT TIME)
ADDRESS STROBE (10/1)
1 KC CLOCK
1 KC DATA
1 KC DATA
1 KC CLOCK
1 KB DATA
NO
COUNT HOLDOFF
COUNT HOLDOFF
ADDRESS VERIFIED
PLATFORM 12.5 KC DATA
1A5A5
ADDRESS
REGISTER
1A5
ADDRESS
SWITCHES
2^0 - 2^{15}
16 LINES
PLATFORM
ADDRESS
CODE
1A5A8 THROUGH 1A5A10
ADDRESS AND DATA
CORRELATOR
ADDRESS VERIFIED
DATA VERIFIED
COUNTHOLDOFF
COUNTHOLDOFF
STOP CLOCK
1A5A6
ERROR
RECOGNIZER
MODE
SWITCH
S17
B1 (1-28 CHAN.
SELECT)
B2 (7-28 CHAN.
SELECT)
B1
B2
B1 (14 DATA LINE CHECK)
B2 (11 DATA LINE CHECK)

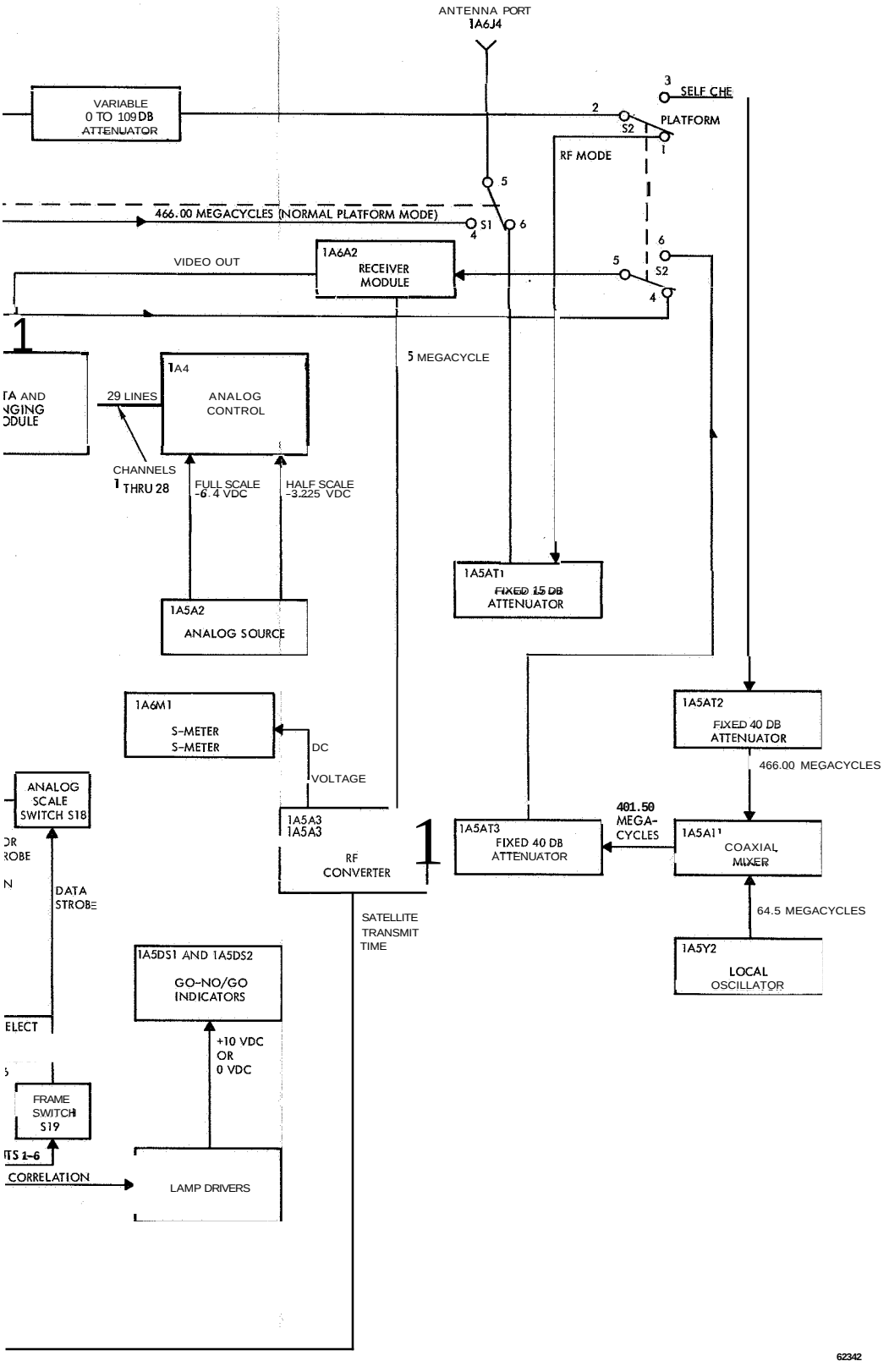


Figure 11. Integration Support Equipment Functional Block Diagram.

data outputs from the range pattern generator to a modulator driver in power control and distribution 1A6A4. These outputs are voltage and impedance level shifted by the modulator driver to derive a DATA MODULATION output to modulate the transmitter. The DATA MODULATION output is hardwired through the 0 position of the MICRO-SEC switch on IRLS time delay simulator 1A3 to transmitter/diplexer 1A6A1. The 466.00 megacycle output from the transmitter is propagated through directional coupler 1A6DC1 to three destinations. This output frequency is provided to COUNTER connector 1A6J2 for frequency measurements, through fixed 20 db attenuator 1A6AT3 to RF POWER connector 1A6J1 for output power monitoring, and contacts 2 and 3 of INITIAL ATTENUATION switch S1. The 30 DB position of switch S1 routs the 466.00 megacycle frequency through fixed 15 db attenuator 1A6AT2 and variable attenuator 1A6AT1 to contacts 2 and 3 of RF MODE switch S2. In this mode, switch S2 routs the transmitter output frequency through fixed 40 db attenuator 1A5AT2 to coaxial mixer 1A5A11 where it is converted to the receiver input frequency of 401.5 megacycles by utilization of the 64.5 megacycle frequency of local oscillator Y2. Fixed 40 db attenuator 1A5AT3 provides additional attenuation to the 401.5 megacycle frequency prior to application through contacts 6 and 5 of RF MODE switch S2 to receiver 1A6A2. The receiver input frequency is amplified, filtered, and mixed to provide a VIDEO OUT signal to data and ranging 1A6A3. At the same time, a 25-megacycle IF signal from receiver 1A6A2 is provided to RF Converter 1A5A3 where it is detected to derive a dc voltage level for signal strength monitoring purposes on S-meter 1A6M1. The RF converter also provides a SATELLITE TRANSMIT TIME and $\overline{\text{SATELLITE TRANSMIT TIME}}$ (via buffers in address register 1A5A5) to event recorder 1A7. A positive dc voltage level representing SATELLITE TRANSMIT TIME will allow event recorder to display the total satellite transmit time.

The VIDEO OUTPUT signal from receiver 1A6A2 is applied to circuits within data and ranging 1A6A3 that regenerates the information content of the signal. In data and ranging 1A6A3, the input data is phase synchronized with internally-regenerated 12.5 KC data and routed to circuits that provide correlation between the incoming platform address code and the hardwired code. When phase synchronization is achieved, the levels of the ERROR THRESHOLD and $\overline{\text{ERROR THRESHOLD}}$ signals (via buffers in range pattern generator 1A5A4) change and are routed to event recorder 1A7 to record the occurrence of phase lock. As phase lock occurs,, the MODULATED DIGITAL SUBCARRIER (12.5 KC DATA) and $\overline{\text{MODULATED DIGITAL SUBCARRIER (12.5 KC DATA)}}$ outputs from data and ranging 1A6A3 are routed through MODE switch S17 to data translator 1A5A7. These inputs are shifted through a delay flip-flop and shift register by the 12.5 KC CLOCK input from range pattern generator at the same time the self-check $\overline{\text{M-WORD}}$ input is being shifted through another counter. These two counter outputs are digitally demodulated to form a clock input to another counter in data translator 1A5A7 that derives the 1 KB DATA output to the address and data correlators. The $\overline{\text{STAGE 1}}$, $\overline{\text{STAGE 2}}$, $\overline{\text{STAGE 3}}$, and STAGE 4 inputs from range pattern generator 1A5A4 are used in data translator 1A5A7 to develop the $\overline{\text{1 KC CLOCK}}$ and $\overline{N_0}$ outputs to the address and data correlators. At this time, the $\overline{\text{COUNT HOLDOFF}}$ logic level is routed through the address and data correlators to error recognizer 1A5A6 to inhibit error recognition circuits.

The $\overline{\text{1 KB DATA}}$ output from data translator 1A5A7 is shifted through an address register by the $\overline{\text{1 KC CLOCK}}$ pulses and applied to a coincidence AND gate for platform address recognition. When the address code is recognized, the address correlator provides an

ADDRESS VERIFIED output to error recognizer 1A5A6 and data translator 1A5A7. This output to error recognizer 1A5A6 has no effect due to the inhibit level of COUNT HOLDOFF. When applied to data translator 1A5A7, the ADDRESS VERIFIED output triggers a flip-flop that generates the MODULATION INVERT COMMAND and COUNT HOLDOFF signals. The MODULATION INVERT COMMAND is provided to range pattern generator 1A5A4 where it initiates development of the platform address code complement (address) as the MODULATED DIGITAL SUBCARRIER and complement outputs through MODE switch S17. The COUNT HOLDOFF signal is provided to error recognizer 1A5A6 where it removes the COUNT HOLDOFF inhibit level, inverts the data, and enables the error recognition circuits. At this time, the DATA MODULATION input to transmitter/diplexer 1A6A1, via IRLS time delay simulator 1A3, represents the platform address code used to modulate the transmitter frequency. Thus, the 466.00-megacycle transmitter-output frequency represents the address code and traverses the identical signal path as the initial address transmission.

When the address code is recognized in data and ranging 1A6A3, the logic level of the FORMAT FLIP-FLOP and the FORMAT FLIP-FLOP outputs from range pattern generator 1A5A4 transit from their preset levels and are provided to event recorder 1A7. The transition of the FORMAT FLIP-FLOP level from a logic ZERO to logic ONE records the time of address recognition and also enables the row and column counters in data and ranging 1A6A3. The source of simulated analog inputs necessary for data frame generation is controlled by the position of CHANNEL switches 1 through 28 an analog control 1A4. The level of each data word input is controlled by ANALOG SCALE S18. Either zero-scale, half-scale, or full-scale levels (0, -3.225, or -6.4 vdc) are programmed through each CHANNEL switch for encoding. Each data line of the output data frame (14 or 11 data lines) contains two 8-bit data words and will be represented by the following zeroscale, half-scale, or full-scale data word codes.

Bit	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
a. Zeroscale:	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
b. Half-scale:	0	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1
c. Full-scale:	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1

The number of data lines checked per data frame is controlled by MODE switch S17 and the number of frames checked per operation is determined by FRAME switch S19. In the 1-28 position, all 14 data lines in a frame are verified while the 7-28 position allows verification of 11 data lines. The latter position is used when the platform-to-be-checked has six hard-wired telemetry point inputs. Verification of up to six data frames can be accomplished by positioning FRAME switch S19.

Prior to actual data word and data line generation, two platform address codes are outputted from range pattern generator 1A5A4 and routed to data and ranging 1A6A3 where they are decoded and verified. Again, the MODULATED DIGITAL SUBCARRIER and MODULATED DIGITAL SUBCARRIER outputs representing 12.5 KC DATA and 12.5 KC DATA are

routed through MODE switch Sf7 to data translator 1A5A7. The data translator demodulates the inputs to 1 KB DATA and applies this output to the address correlators. The 1 KB DATA representing the two address codes are AND'd with the unique N-Word and decoded and the resulting two ADDRESS VERIFIED pulses are provided to error recognizer 1A5A6 for storage in an error counter.

When data frame generation is initiated, the preprogrammed CHANNEL 1 through 28 inputs from analog source 1A5A2 are routed through analog control 1A4 and sequentially applied through channel and frame gates in data and ranging 1A6A3 to an analog-to-digital converter (A/D) for encoding. The A/D converter accepts each channel input and encodes the simulated analog transducer voltage into an eight-bit digital word. These encoded words are shifted through the latter stages of the address register in data and ranging 1A6A3 as a 1 KC data stream and modulated with 12.5 KC regenerated range word data to generate the MODULATED DIGITAL SUBCARRIER and complement outputs to data translator 1A5A7. Again, the data translator demodulates these inputs into 1 KB DATA for application to the data correlator. As each data line (two data words) is verified, the correlator generates a DATA VERIFIED pulse output to an error counter in error recognizer 1A5A6. If MODE switch S17 is in the 1-28 position, 14 data lines (28 data words) will be verified and the switch selects the B1 output for error detection. If MODE switch S17 is in the 7-28 position, 11 data lines (22 data words) will be verified and the switch selects the B2 output for error detection. After the last data line has been verified, a third address code is recognized in the address correlator and a third ADDRESS VERIFIED pulse is provided to an address error counter in error recognizer 1A5A6. The states of the address and data error counters are detected in order to develop a frame pulse output to the frame counter. If the correct number of data frames have been transmitted, as determined by FRAME switch S19, a FRAME CORRELATION output causes lamp drivers 1A5A2 to energize GO indicator 1A5DS2. If the proper number of address codes, data lines, and frames are not verified, no FRAME CORRELATION pulse will be generated and NO GO indicator 1A5DS1 will be energized.

3-5. Directly Cabled Or Close Proximity Mode.

In order for the ISE to operate in the directly cabled or close proximity mode, INITIAL ATTENUATION switch S1 must be in the 30 DB position, RF MODE switch in the PLATFORM position, and self-check MODE switch S17 in the PLATFORM position, The 1 through 28 CHANNEL switches on analog control 1A4 must also be programmed to select an external or internal simulated transducer voltage. If internal, ANALOG SCALE switch S18 must be positioned to the selected voltage scale. During satellite interrogation, these switch positions rout the satellite transmitter output through the correct signal path and allow encoding of channel data for transmission. The 401.5 megacycle input frequency entering ANTENNA PORT connector 1A6J1 is passed through contacts 5 and 6 of INITIAL ATTENUATION switch S1, fixed 15 db attenuator 1A5AT1, and contacts 1 and 2 of RF MODE switch S1 to low-power attenuator 1A6AT1. This attenuator provides a variable 0 to 109 db attenuation of ISE and satellite transmitter power output. The attenuated signal from variable attenuator 1A6AT1 passes through fixed 15 db attenuator 1A6AT2 and contacts 2 and 3 of INITIAL ATTENUATION switch S1 to directional coupler 1A6DC1. One output from the coupler is routed to RF POWER connector 1A6J1 for power measurements and a second output is routed to COUNTER connector 1A6J2 for frequency measurements. The 401.5 megacycle output from directional

coupler 1A6DC1 is also routed through the diplexer in transmitter/diplexer 1A6A1 and contacts 4 and 5 of RF MODE switch S2 to receiver 1A6A2. The receiver input frequency is amplified, filtered, and mixed to provide a VIDEO OUT signal to data and ranging 1A6A3. Receiver 1A6A2 also provides a 25 megacycle IF signal to RF converter 1A5A3 where it is detected to derive a dc voltage level for power monitoring on S-meter 1A6M1 and a positive SATELLITE TRANSMIT TIME level to event recorder 1A7 and address register 1A5A5. The input to address register 1A5A5 is buffered and inverted and applied to event recorder 1A7 as a SATELLITE TRANSMIT TIME level. The direct SATELLITE TRANSMIT TIME input from RF converter 1A5A3 initiates recording of satellite transmitter on time.

The VIDEO OUT signal from receiver 1A6A2 is applied to data and ranging 1A6A3 where the information content is regenerated and synchronized. The phase synchronized and regenerated 12.5 KC data and decommutated 1 KC data are applied to an address correlator circuit that compares the incoming platform address code with the address hardwired in the correlator. Detection of a correct address code develops the ADDRESS SYNC output to power control and distribution 1A6A4. The ADDRESS SYNC pulse activates a relay in power control and distribution 1A6A4 which generates the TRANSMITTER ON command to transmitter/diplexer 1A6A1 and also removes an inhibit level of the TELEMETRY HOLDOFF signal from the formatting circuits and three-second counter in data and ranging 1A6A3. The transition from logic ZERO to logic ONE of the TELEMETRY HOLDOFF signal is also routed to event recorder 1A7 to physically display the time of address recognition and to range pattern generator 1A5A4 for inversion and application to the recorder as TELEMETRY HOLDOFF.

The decommutated 1 KC data output from the platform address register is modulated with the internally regenerated 12.5 KC range-word data to generate the MODULATED DIGITAL SUBCARRIER and MODULATED DIGITAL SUBCARRIER outputs. These outputs are routed through the PLATFORM position of MODE switch S17 to a modulator driver in power control and distribution 1A6A4. The modulator driver level shifts the voltage and impedance of the signal to the levels required to modulate the transmitter. The DATA MODULATION output from power control and distribution 1A6A4 is hardwired through the 0 position of the MICRO-SEC switch on IRLS time delay simulator 1A3 directly to transmitter/diplexer 1A6A1. Positions 1280 through 2000 of the MICRO-SEC switch program simulated propagation delays of satellite-to-platform transmissions. The 466.00 megacycle output frequency from transmitter/diplexer 1A6A1 is routed through contacts 2 and 3 of INITIAL ATTENUATION switch S1, attenuator 1A6AT2 and 1A6AT1, contacts 1 and 2 of RF MODE switch S2, attenuator 1A5AT1, and contacts 5 and 6 of INITIAL ATTENUATION switch S1 to ANTENNA PORT connector 1A6J4. Thus, the platform address code, generated in the satellite, is received and detected in the ISE platform and returned unchanged to the satellite.

The satellite responds to the ISE transmission by repeatedly transmitting the platform address complement code (address) back to the platform. The incoming transmission representing the address code is routed over the identical signal path of the initial transmission. When the address code is detected in data and ranging 1A6A3, the level of the FORMAT FLIP-FLOP changes from a logic ZERO to a logic ONE, thus indicating address correlation. This transition removes preset inhibit levels from the column and frame counters in data and ranging 1A6A3 and prepares the formatting logic for data frame generation. The FORMAT FLIP-FLOP signal is routed through power control and distribution 1A6A4 to range pattern

generator 1A5A4. It is buffered and outputted to event recorder 1A7 as the FORMAT FLIP-FLOP logic ONE level to enter the time of address recognition. The signal is also inverted in range pattern generator 1A5A4 and provided to event recorder 1A7. Also at this time, if the input signal and regenerated data has not been phase synchronized, the level of the ERROR THRESHOLD signal remains at logic ZERO and the data output from data and ranging 1A6A3 is inhibited. When phase synchronization occurs, ERROR THRESHOLD transits from logic ZERO to logic ONE and is routed through power control and distribution 1A6A4 and range pattern generator 1A5A4 to event recorder 1A7. The exact time of synchronization is recorded in this manner.

Data frame generation is initiated after address correlation and data synchronization. Prior to data word development, two address codes are transmitted from the ISE platform to prepare the satellite for data frame reception. The CHANNEL switches on analog control 1A4 determine whether or not each data word in the output data frame will be programmed from an external precision source or transducer or internally from analog source 1A5A2. All CHANNEL (data word) inputs are sequentially routed to an analog-to-digital converter in data and ranging 1A6A3 where they are changed from an analog voltage to a digital word. These digital words are loaded and shifted through the platform address register as 1 KC data. Again, the 1 KC data is modulated with 12.5 KC regenerated range word data to generate the MODULATED DIGITAL SUBCARRIER and complement outputs to MODE switch S17. The MODE switch routs the modulated outputs through a modulator driver in power control and distribution 1A6A4. The DATA MODULATION signal is routed to transmitter/diplexer 1A6A1 via IRLS time delay simulator 1A3 for transmission to the satellite. The FRAME switch **(519)** determines the number of data frames transmitted to the satellite. If more than one frame is to be transmitted, the data content of the additional frames will be identical to the first frame if the source does not change. At the end of the last data frame transmitted, the END OF FRAME output from data and ranging 1A6A3 activates a relay in power control and distribution 1A6A4 that generates the TRANSMITTER OFF command. If data frame transmission is not completed within three seconds, the END OF 3 SECONDS output from data and ranging 1A6A3 will activate the same relay in power control and distribution 1A6A4 and generate the TRANSMITTER OFF command.

3-6. Normal Satellite-To-Platform Mode.

Operation of the ISE in the normal satellite-to-platform mode is similar to that of the directly cabled or close proximity mode. With exception of initial and final signal flow, the functional sequences and operations are identical. To operate correctly in this mode, INITIAL ATTENUATION switch S1 must be in the 0 DB position, RF MODE switch must be in the PLATFORM position, VERNIER ATTENUATION control 1A6AT1 must indicate 0 db, and MODE switch S17 must be in the PLATFORM position. As shown in Figure 11, these switch positions permit direct routing of transmitted or received frequencies entering ANTENNA PORT connector 1A6J4 without additional attenuation. In this mode, a suitable GFE antenna must be attached to ANTENNA PORT connector 1A6J4.

3-7. PLATFORM FUNCTIONAL DISCUSSION.

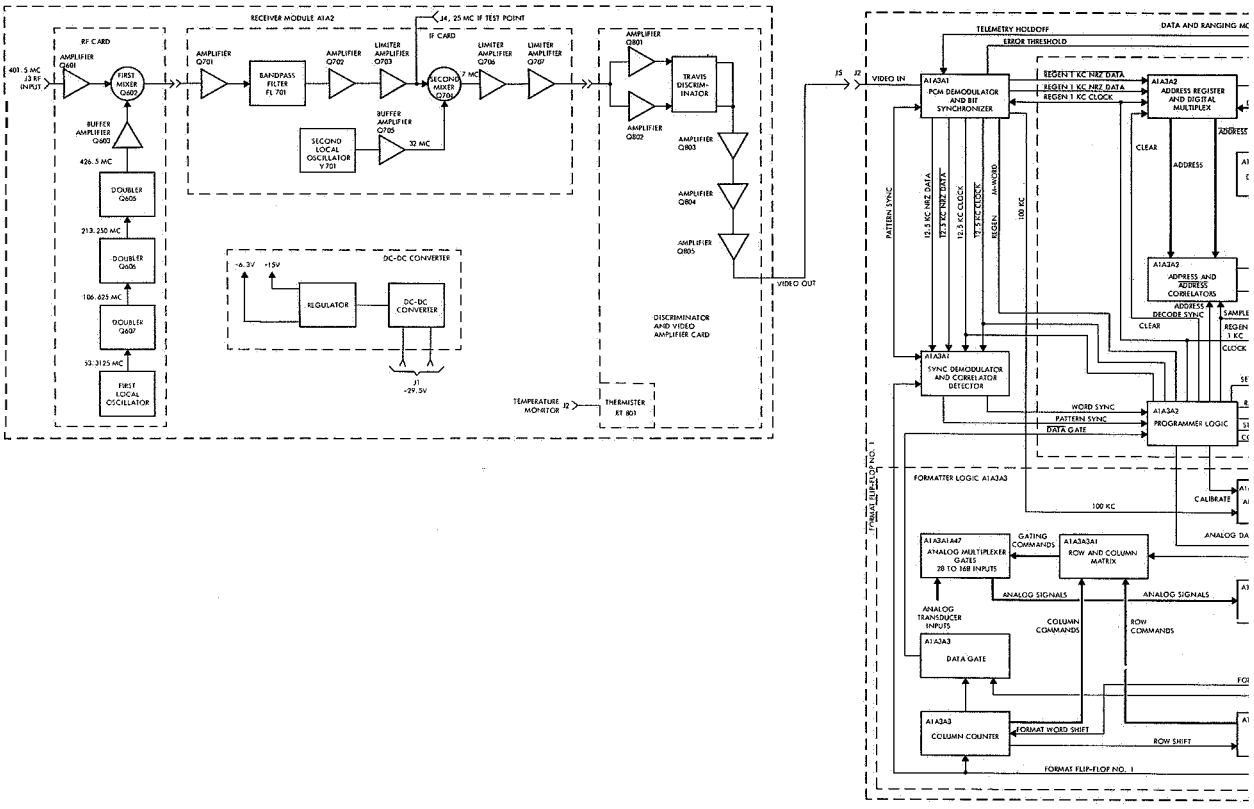
3-8. General.

The function of the Platform Equipment is to accept individual analog voltage inputs between 0 and -6.4 volts from 28 to 168 transducer sensing devices and encode and multiplex these inputs into a seven bit digital word. After analog-to-digital conversion, the logic circuits in the platform insert the converted information into one to six data frames comprised of 28 data words each. The data frames are modulated with a 12.5 KC subcarrier frequency and applied to the transmitter input for transmission to the satellite.

The block diagram of the Platform Equipment is illustrated in Figure 12. This unit is comprised of four individual module assemblies located in RF control 1A6 which may be further subdivided as shown in the block diagram. These modules include transmitter module A1, receiver module A2, data and ranging module A3, and power control and distribution module A4. Functional circuits within transmitter module A1, supplied by TRW Space Laboratories, are comprised of an amplifier driver, power amplifier, diplexer, power supply, and temperature monitoring transducers. The receiver module (A2) is also provided by TRW Space Technology Laboratories and is comprised of RF and IF sections, a power supply, and a discriminator and video output amplifier. Data and ranging module A3 includes printed-circuit cards that contain functional circuits pertaining to the PCM demodulator and bit synchronizer, sync demodulator and correlator detector, platform logic, and formatter logic. Power control and distribution module A4 is comprised of a dc-to-dc converter, modulator driver, and relay control circuits. A block diagram analysis for each functional area is discussed in the following paragraphs. When referring to Figure 12, disregard reference designator A1 that prefixes all module and submodule designators. Reference designator A1 applies only to the platform equipment as identified with the platform housing. As the platform modules are part of RF control 1A6, reference designator 1A6 should prefix the designators shown.

3-9. Receiver Module A2.

The 401.5 megacycle PCM/FM output from the diplexer section of transmitter module A1 or mixer 1A5A11 is applied to the RF section of receiver module A2 through RF INPUT connector A2J3 and routed through a low-noise amplifier to the first mixer stage of the receiver. The crystal-controlled local oscillator in the RF section operates at its fifth overtone and provides an output frequency of 53.3125 megacycles to the first common-emitter doubler whose collector tank circuit is tuned to 106.625 megacycles. This frequency is again doubled by a second common emitter doubler to achieve a frequency of 213,250 megacycles. A frequency of 426.5 megacycles from the third doubler is routed through a buffer amplifier to the second input of the first mixer stage where a difference frequency of 25 megacycles is derived. The 25 megacycle difference frequency is applied through an internal connection to the receiver IF section. The 25 megacycle input to the IF section is amplified by a common-emitter amplifier and applied to a crystal bandpass filter. This filter determines the 25 megacycle IF bandwidth which is applied to the second amplifier stage. The output frequency from the limiter amplifier provides the necessary input to the second receiver mixer and also a 25 megacycle output to a receiver test point and RF converter A3 in self check 1A5. The


RECEIVER MODULE A1A2
RF CARD
IF CARD
401.5 MC (3 RF INPUT)
AMPLIFIER Q601
FIRST MIXER Q602
BUFFER AMPLIFIER Q603
426.5 MC
DOUBLER Q605
213.250 MC
DOUBLER Q606
106.625 MC
DOUBLER Q607
53.3125 MC
FIRST LOCAL OSCILLATOR
AMPLIFIER Q701
BANDPASS FILTER FL 701
AMPLIFIER Q702
LIMITER AMPLIFIER Q703
SECOND MIXER Q704
7 MC
LIMITER AMPLIFIER Q706
LIMITER AMPLIFIER Q707
14.25 MC IF TEST POINT
BUFFER AMPLIFIER Q705
SECOND LOCAL OSCILLATOR Y 701
32 MC
DC-DC CONVERTER
-6.3V +15V
REGULATOR
DC-DC CONVERTER
J1
-29.5V
AMPLIFIER Q801
AMPLIFIER Q802
TRAVIS DISCRIMINATOR
AMPLIFIER Q803
AMPLIFIER Q804
AMPLIFIER Q805
DISCRIMINATOR AND VIDEO AMPLIFIER CARD
VIDEO OUT
TEMPERATURE MONITOR
THERMISTER RT 801
J5
J2
VIDEO IN
TELEMETRY HOLDOFF
ERROR THRESHOLD
A1A3A1 PCM DEMODULATOR AND BIT SYNCHRONIZER
REGEN 1 KC NRZ DATA
REGEN 1 KC NRZ DATA
REGEN 1 KC CLOCK
A1A3A2 ADDRESS REGISTER AND DIGITAL MULTIPLEX
CLEAR
ADDRESS
PATTERN SYNC
12.5 KC NRZ DATA
12.5 KC NRZ DATA
12.5 KC CLOCK
12.5 KC CLOCK
REGEN
44-WORD
100 KC
A1A3A2 ADDRESS AND ADDRESS CORRELATORS
ADDRESS DECODE SYNC
CLEAR
A1A3A1 SYNC DEMODULATOR AND CORRELATOR DETECTOR
WORD SYNC
PATTERN SYNC
DATA GATE
A1A3A2 PROGRAMMER LOGIC
FORMATTER LOGIC A1A3A3
CALIBRATE
100 KC
A1A3A1A7 ANALOG MULTIPLEXER GATES 28 TO 168 INPUTS
GATING COMMANDS
A1A3A3A1 ROW AND COLUMN MATRIX
ANALOG SIGNALS
ANALOG SIGNALS
ANALOG TRANSDUCER INPUTS
COLUMN COMMANDS
ROW COMMANDS
A1A3A3 DATA GATE
A1A3A3 COLUMN COUNTER
FORMAT WORD SHIFT
ROW SHIFT
FORMAT FLIP-FLOP NO. 1

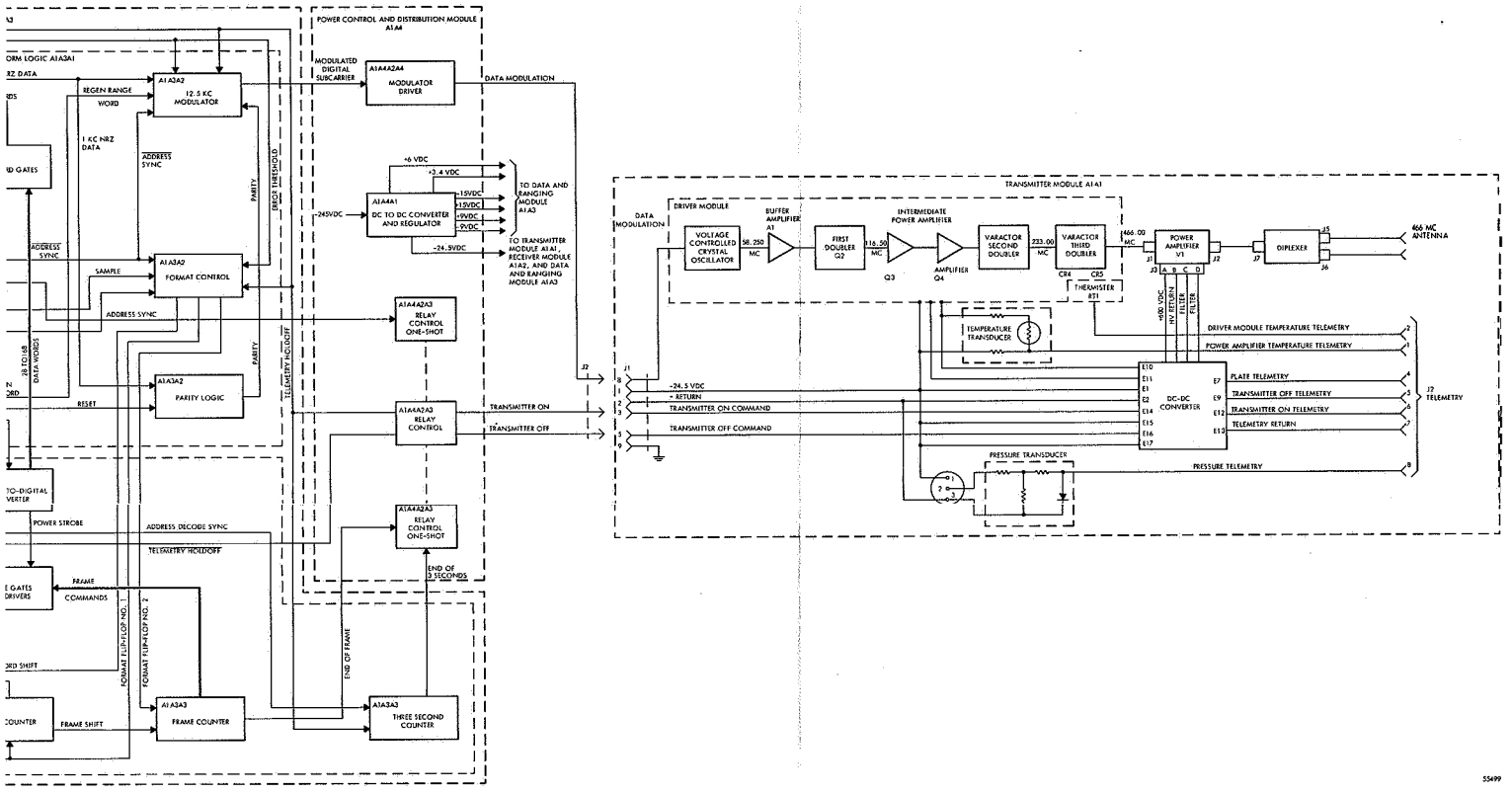


Figure 12. Platform Functional Block Diagram.

25 megacycle input to the second mixer is combined with the buffered 32 megacycle output from the crystal-controlled local oscillator in the IF section to derive a difference frequency of 7 megacycles. The 7 megacycle difference frequency is amplified by two limiter amplifiers and applied through an internal connection to the discriminator and video amplifier section. The 7 megacycle input is amplified and applied to the two inputs of the stagger tuned Travis Discriminator. The discriminator provides an output amplitude proportional to the instantaneous frequency excursion of the receiver input from the carrier frequency which represents the input modulation. The discriminator output is amplified and provided to data and ranging module A3 through receiver connector A2J3.

3-10. Data And Ranging Module A3.

3-11. PCM Demodulator and Bit Synchronizer A3A1A1.

The function of PCM demodulator and bit synchronizer A3A1 is to accept the video output from receiver A2 and regenerate the information content of the received signal. Regeneration of the information content is accomplished by first producing a 100 KC output from the receiver input and then demodulating the 100 KC in order to produce a 1 KC data stream and 12.5 KC clock pulses. Phase synchronization between the received input and the regenerated data is also accomplished in this unit. The PCM demodulator and bit synchronizer receives inputs from receiver A2, platform logic A3A2, the sync demodulator and correlatar detector, and power control and distribution module A4. The inputs and their functional areas are as follows:

Functional Area	input
Receiver A2	1. Video Input.
Platform Logic A3A2	1. Regenerated 1 KC clock. 2. Regenerated M-word.
Sync Demodulator and Correlator Detector A3A1	1. Pattern sync.
Power Control and Distribution Module A4	1. Telemetry holdoff.

Outputs from the PCM demodulator and bit synchronizer and their associated functional areas are as follows:

Functional Area	Output
Platform Logic A3A2	1. Regenerated 1 KC NRZ data. 2. Regenerated 1 KC NRZ data. 3. 12.5 KC clock. 4. 12.5 KC clock.

Functional Area	output
Sync Demodulator and Bit Synchronizer	1. 12.5 KC NRZ data. 2. 12.5 KC NRZ data. 3. 12.5 KC clock. 4. 12.5 KC clock.
Formatter Logic A3A3	1. 100 KC clock.

The PCM demodulator and bit synchronizer contains circuits that function to demodulate the receiver input to produce a 100 KC pulse train, regenerate the 12.5 KC data information of the video signal, count down the 100 KC pulse train to provide the 12.5 KC clock pulses, and to provide phase synchronization between the receiver input and the regenerated M-word from platform logic A3A2.

The PCM demodulator and bit synchronizer accepts the video input from receiver A2 and transformer couples this input to the 12.5 KC regeneration circuits, to the phase detection circuits, and the circuits that demodulate the input to provide the 100 KC output. Phase synchronization in the PCM demodulator and bit synchronizer begins upon reception of the receiver input and is achieved when the regenerated 12.5 KC is detected and locked onto the input phase. The 100 KC output is utilized internally to derive the 12.5 KC and 12.5 KC CLOCK pulse outputs to the sync demodulator and correlator detector. The 12.5 KC CLOCK output is utilized to shift the 12.5 KC NRZ DATA and 12.5 KC NRZ DATA through a 12-stage shift register while the 12.5 CLOCK strobes the correlators to generate the WORD SYNC and PATTERN SYNC outputs. The 100 KC output is also provided to the analog-to-digital converter in formatter logic A3A3 as a clock pulse input to an encoding binary counter. The REGENERATED M-WORD input from platform logic A3A2 is utilized to perform a serial correlation between the receiver input in order to determine the binary value of each input range word. The REGENERATED 1 KC CLOCK input, generated concurrently with the REGENERATED M-WORD, reads the REGENERATED 1 KC NRZ DATA and REGENERATED 1 KC NRZ DATA out *of* the PCM demodulator and bit synchronizer and through the address and address correlators. The ERROR THRESHOLD logic level output is a function of the phase detection circuits. If the error threshold voltage is at a logic ZERO level, it indicates that phase synchronization between the receiver input and the regenerated data has not been achieved and that data frame transmission cannot be initiated. This logic ZERO level disables the 12.5 KC Modulator and sets a data disable flip-flop to inhibit the formatter logic. If the ERROR THRESHOLD level is a logic ONE, phase synchronization has been achieved and, if ADDRESS SYNC is recognized, data frame encoding and transmission is immediately initiated. The PATTERN SYNC input from the sync demodulator and correlator detector enables the phase detection circuits which, in turn, provides the error threshold level. The TELEMETRY HOLDOFF input from power control and distribution module A4 provides preset levels for the phase detection circuits until the following interrogation or equipment operation.

3-12. Sync Demodulator and Correlator Detector A3A1.

The function of the sync'demodulator and correlator detector is to accept the 12.5 KC NRZ DATA and its complement and to analyze the content *of* this data to determine the minor bit composition of the range word pattern. Upon correlation of the input data, the

sync demodulator and correlator detector provides the synchronization signals necessary for proper system operation. The sync demodulator and correlator detector receives inputs from PCM demodulator and bit synchronizer A3A1 and platform logic A3A2. The inputs and their functional areas are as follows:

Functional Area	input
PCM Demodulator and Bit Synchronizer A3A1	1. 12.5 KC NRZ data. 2. $\overline{12.5 \text{ KC NRZ data}}$. 3. 12.5 KC clock. 4. $\overline{12.5 \text{ KC clock}}$.
Platform Logic A3A2	1. Format Flip-flop No. 1

Outputs from the sync demodulator and bit synchronizer and their functional areas are as follows:

Functional Area	output
Platform Logic A3A2	1. Word sync. 2. Pattern sync.

The sync demodulator and bit synchronizer consists of circuits that function as a 12-stage shift register and control gates that perform a correlation with the input 12.5 KC data in order to produce the word and pattern synchronizing signals to the platform logic.

The range word pattern input to the sync demodulator and correlator detector consists of the 12.5 KC NRZ DATA outputs from PCM demodulator and bit synchronizer A3A1. This data consists of 12 minor bits that comprise an eight minor bit M-word and a four-minor bit N-word. The bit value of each minor bit that comprise the M-word will be 10101100 when the overall range word is to have a binary ONE value. The minor bit value of the M-word when the overall range word is to have a binary ZERO value is 01010011 or $\overline{M}$. The minor bit value of the four bit N-word will always be 1001 except when the input range word is the first range word in the platform address. For this range word input, the minor bit value of the N-word will be 0110 or $\overline{N}$. The correlator detects the presence of the eight minor bit M or $\overline{M}$ word and the four minor bit N or $\overline{N}$ word to produce the synchronizing outputs.

The 12.5 KC NRZ DATA and $\overline{12.5 \text{ KC NRZ DATA}}$ input from PCM demodulator and bit synchronizer A3A1 is shifted serially into the 12-stage shift register by the 12.5 KC CLOCK pulses. When the shift register is loaded with the eight minor bit M or $\overline{M}$ word and four minor bit N or $\overline{N}$ word, the $\overline{12.5 \text{ KC CLOCK}}$ pulse from the PCM demodulator and bit synchronizer strobes the correlator control gates to detect the presence of the M or $\overline{M}$ or N or $\overline{N}$ word. The WORD SYNC output from the sync demodulator and correlator detector occurs when the eight minor bit M or $\overline{M}$ word and four minor bit N or $\overline{N}$ word is in the shift register and therefore, occurs during each range word interval. The PATTERN SYNC output occurs when the eight minor bit M or $\overline{M}$ word and the four minor bit $\overline{N}$ word is in the shift register and therefore, occurs once every 16 range words. The FORMAT FLIP-FLOP No. 1

input to the sync demodulator and correlator detector occurs after platform address recognition and functions to inhibit the correlation of the four minor bit N or $\overline{N}$ word and therefore, inhibits generation of both the WORD SYNC and PATTERN SYNC outputs.

3-13. Platform Logic A3A2.

The function of platform logic A3A2 is to determine that the platform address transmitted by the satellite is correct and when address recognition has occurred, generate the proper timing and format control signals that allow the encoded analog data from formatter logic A3A3 to be processed and transmitted.

The platform logic contains operational circuits that function as the 17-stage address register and digital multiplexer, address and address complement correlators, programmer logic, parity logic, format control logic, 12.5 KC modulator, and data word input gates. Inputs to the platform logic are received from PCM demodulator and bit synchronizer A3A1, sync demodulator and correlator detector A3A1, formatter logic A3A3, and power control and distribution module A4. The inputs and their associated functional area are as follows:

Functional Area	Input
PCM Demodulator and Bit Synchronizer A3A1	1. Regenerated 1 KC NRZ data. 2. $\overline{\text{Regenerated 1 KC NRZ data.}}$ 3. Error threshold. 4. 12.5 KC clock. 5. $\overline{\text{12.5 KC clock.}}$
Sync Demodulator and Correlator Detector A3A1.	1. Word sync. 2. Pattern sync.
Formatter Logic A3A3	1. $\overline{\text{Data}}$ gate. 2. 28 to 168 data words.
Power Control and Distribution Module A4	1. Telemetry holdoff. 2. Operating voltages.

Outputs from the platform logic and their associated functional areas are as follows:

Functional Area	output
PCM Demodulator and Bit Synchronizer A3A1	1. Regenerated 1 KC clock. 2. Regenerated M-word.
Formatter Logic A3A3	1. Calibrate level. 2. Code level. 3. Strobe level. 4. Format word shift. 5. Format flip-flop No. 1. 6. Format flip-flop No. 2.

Functional Area	output
Power Control and Distribution Module A4	1. Modulated digital subcarrier. 2. Address sync.

A counter in the programmer logic accepts the 12.5 KC CLOCK pulse input from PCM demodulator and bit synchronizer A3A1 and the WORD SYNC input from sync demodulator and correlator detector A3A1 and generates a 1 KC CLOCK pulse output, REGENERATED RANGE WORD, REGENERATED M-WORD, and a SAMPLE pulse. The REGENERATED M-WORD is routed to PCM demodulator and bit synchronizer where a correlation is performed with the receiver input to determine the binary bit value of each 1 KC range word. The 1 KC CLOCK pulses are utilized to read the 1 KC NRZ DATA out of the PCM demodulator and bit synchronizer. The SAMPLE pulse output from the programmer logic is provided to the address and address correlators and format control to be utilized as a strobe pulse.

The 1 KC CLOCK pulses are also utilized internally within the programmer logic to drive another counter that counts the number of 1 KC bits (range words) in the received address code. This counter is reset by the PATTERN SYNC pulse from sync demodulator and correlator detector A3A1 which occurs during the presence of the first range word in the address register and digital multiplexer. When the ADDRESS or $\overline{\text{ADDRESS}}$ occupy the first 16 stages of the 17-stage shift register in the address register and digital multiplexer, this counter produces the ADDRESS DECODE SYNC pulse that is utilized to strobe the address and address correlators and to drive the three-econd counter in formatter logic A3A3. In addition to the above outputs, this particular counter in the programmer logic generates the CALIBRATE, CODE, and STROBE commands to analog-to-digital converter A3A1A46, the parity logic RESET pulse, and the CLEAR and SET pulses utilized to insert encoded data words into the address register and digital multiplexer.

The 1 KC CLOCK pulses from the programmer logic is applied to the address register and digital multiplexer where they are utilized to shift the 1 KC NRZ DATA from PCM demodulator and bit synchronizer A3A1 through the register. When the first 16 stages of the address register and digital multiplexer are loaded, a comparison between the hardwired address and the incoming ADDRESS is performed by the address and address correlators. The correlators are strobed at the correct time by the ADDRESS DECODE SYNC pulse from the programmer logic to ensure against false synchronization due to incorrect data and additionally strobed by the programmer logic SAMPLE pulse in the middle of the range word to ensure against false synchronization due to switching transients.

The prgsence of a correct ADDRESS achieves correlation, which in turn, generates the ADDRESS SYNC pulse output from the address and address correlators. The logic level of the ADDRESS SYNC pulse triggers a one shot in relay control A4A2A3 which allows a relay in relay control A4A2A3 to energize. Operation of the relay supplies a TRANSMITTER ON command to transmitter module 1A6A1. Another set of relay contacts are opened and removes a TELEMETRY HOLDOFF preset voltage from PCM demodulator and bit synchronizer A3A1, formatter logic A3A3, and the format control and 12.5 KC modulator in platform logic 1A6-A3A2. At this time, the 1 KC CLOCK pulses from the programmer logic continues to shift the 1 KC DATA through the 17-stage shift register in the address register and digital multi-

plexer. The 1 KC output from the register is routed to the 12.5 KC modulator where it is modulated with the REGENERATED RANGE WORD output from the programmer logic to produce a MODULATED DIGITAL SUBCARRIER for application to the modulator driver.

When the satellite receives the unchanged platform address, it immediately transmits the platform address complement (address) back to the platform. When the complete ADDRESS code is shifted into the first T6-stages of the address register and the digital multiplexer, the address and address correlators generate the ADDRESS SYNC pulse output to the format control and 12.5 KC modulator. If phase synchronization has not been obtained in PCM demodulator and bit synchronizer A3A1 (indicated by the logic level of the ERROR THRESHOLD signal), the ADDRESS SYNC pulse sets a flip-flop in format control that inhibits the 1 KC DATA output from the address register and digital multiplexer. Instead, the address register output will consist of modulated data stream of binary ONES until phase synchronization has been achieved. If phase synchronization has been achieved, the address sync pulse sets another flip-flop in format control that enables the 1 KC CLOCK pulses from the programmer logic to continuously shift the 1 KC DATA through the address register and digital multiplexer. Setting this flip-flop allows the format control to provide enable levels to the frame, row, and column counters in formatter logic A3A3 and an inhibit level to cease generation of WORD and PATTERN SYNC pulses from sync demodulator and correlator detector A3A1. It also enables the format control gate that provides the FORMAT WORD SHIFT pulse to the column counter in formatter logic 1A6A3A3.

Prior to data frame generation, the format control supplies three FORMAT WORD SHIFT pulses to the column counter in formatter logic A3A3 while two ADDRESS codes are being shifted through the address register and digital multiplexer. When the formatter logic column counter receives the fourth FORMAT WORD SHIFT pulse (mid-point of second ADDRESS code), a DATA GATE pulse is generated in formatter logic A3A3 and applied to the programmer logic in platform logic A3A2. This enables the programmer logic gates that generate the register CLEAR pulse output to the address register and digital multiplexer and the data SET pulse output to the data word gates. The parity logic is also reset at this time. The CLEAR pulse output from the programmer logic presets stages 9 through 16 of the address register and digital multiplexer causing binary ZEROS to appear at their outputs. The SET pulse output from the programmer logic strobes the data word gates and allows the 7-binary bit digital word generated by the analog-to-digital converter to be loaded broadside into stages 10 through 16 of the address register and digital multiplexer.

After loading, the following 1 KC CLOCK pulse shifts the first 1 KC DATA bit (range word) into the output stage of the address register and digital multiplexer where it is converted into a RZ format and presented to the 12.5 KC modulator and parity logic. The remaining 1 KC DATA bits are then shifted out of the address register and digital multiplexer in a normal manner followed by a binary ZERO bit value. At this time, the CLEAR and RESET output from the programmer logic again occurs and the second 7-bit data word is shifted out of the address register followed by a binary ZERO. At the termination of every even data word, the parity logic inserts its contents into the data bit stream as the parity bit and the parity logic is reset by the programmer logic.

The above platform logic sequence is continuous until 28 DATA WORDS for one data frame has been shifted out of the address register and digital multiplexer. When the last parity bit per frame has been read out, the $\overline{\text{DATA GATE}}$ output from formatter logic A3A3 is removed and data insertion through the data word gates in inhibited. At this time, one platform $\overline{\text{ADDRESS}}$ is shifted through the address register and digital multiplexer to terminate platform transmission.

3-14. Formatter Logic A3A3.

The function of formatter logic A3A3 is to accept incoming data in the form of analog voltages from transducer sensing devices and/or the analog source in self-check 1A5 (via analog control 1A4), position this information in the correct data word and data frame position, and encode the data into a 7-bit digital word for processing and transmission. Timing signals for termination of platform transmission is also a function of the formatter logic. The formatter logic contains operational circuits that function as the analog-to-digital converter, row, column, and frame counters, analog multiplexer gates, analog multiplexer matrix, three second counter, data enable gate, and frame gates and drivers. The formatter logic receives inputs from PCM demodulator and bit synchronizer A3A1, platform logic A3A2, power control and distribution module A4, and the analog transducer sensing devices or analog source. The inputsand their associated functional area are as follows:

Functional Area	Input
PCM Demodulator and Bit Synchronizer A3A1	1. 100 KC clock.
Platform Logic A3A2	1. Calibrate level. 2. Code level. 3. Strobe level. 4. Address decode sync. 5. Format word shift. 6. Format flip-flop No. 1. 7. Format flip-flop No. 2. 8. 1 KC clock.
Power Control and Distribution Module A4	1. Telemetry hold off. 2. Operating voltages. 3. $\overline{\text{Telemetry hold off}}$.
Analog Control	1. Simulated transducer analog inputs.

Outputs from the formatter logic and their associated functional areas are as follows:

Functional Area	output
Platform Logic A3A2	1. $\overline{\text{Data gate}}$. 2. 28 to 168 seven bit digital data words. 3. Error threshold.

Functional Area	output
Power Control and Distribution Module A4	1. End of frame. 2. End of 3 seconds.

Prior to actual data word and data frame generation and encoding, the column and row counters in the formatter logic are held in a preset state by the FORMAT FLIP-FLOP No. 1 input from the format control in platform logic A3A2. The frame counters are held in a preset state by the FLIP-FLOP No. 2 input that is also from the format control in platform logic A3A2. The TELEMETRY HOLDOFF input from the relay control in power control and distribution module A4 inhibits operation of the threesecond counter. In the operational sequence, the three-second counter is enabled by the removal of the TELEMETRY HOLDOFF signal when the address and address correlators recognize the platform address code and generates the ADDRESS SYNC pulse. The ADDRESS DECODE SYNC pulse is counted by this counter in order to produce an END-OF-THREE SECONDS pulse, to deenergize the transmitter, in the event that the END-OF-FRAME pulse from the frame counter does not appear.

When the address and address correlators in platform logic A3A2 recognize the address transmission from the satellite or self check, an ADDRESS SYNC pulse resets a flip-flop in the format control which removes the FORMAT FLIP-FLOP No. 1 preset condition from the row and column counters and allows them to be advanced by FORMAT WORD SHIFT pulses. The frame counters are also enabled by removal of the FORMAT FLIP-FLOP No. 2 preset condition. The FORMAT WORD SHIFT pulses are generated during range word eight and sixteen of each platform address by utilization of the SAMPLE pulse in the platform logic format control. The FORMAT WORD SHIFT pulses are applied to the column counter and allows the counter to advance at eight range word intervals of the continuously transmitted platform address code. After application of a FORMAT WORD SHIFT pulse, the column counter provides a column command to the row and column matrix which, in turn, generates a GATING COMMAND to the analog multiplexer gates to sample one analog input. After generation of five such column commands, the column counter also produces a row shift pulse output to the row counter. The row counter supplies row commands to the row and column matrix in order to position the sampled analog inputs in the correct row with respect to the proper column. The row counter (in conjunction with the frame counter) also provides a frame shift pulse for application to the frame counter. The number of data frames to be encoded and transmitted is governed by the frame counter. This counter provides FRAME COMMANDS to the frame gates and drivers in order to properly position the sampled analog inputs in the correct data frame, and, after frame generation is complete, provides an END-OF-FRAME pulse to the relay control one shot to turn off the transmitter and reapply the preset voltages.

There may be as many as six sets of 28 analog multiplexer gates, one set for each data frame that may be encoded and transmitted. Each analog input may be sampled upon generation of the GATING COMMANDS from the row and column matrix. These analog signals are routed to the frame gates and drivers, controlled by the frame counter, to select the proper data frame information to be supplied to the analog-to-digital converter for encoding. The POWER STROBE input to the frame gates and drivers is applied in response to the STROBE command to the analog-to-digital converter from the programmer logic in platform logic A3A2. This command permits the 28 sampled analog signals to be presented to the analog-to-digital

converter for encoding. Upon application of the CODE command from the programmer logic in pldtform logic A3A2, the analog-to-digital converter encodes the sampled analog data into a seven-binary bit digital word and applies these encoded bits to the data gates in platform logic A3A2. Prior to this occurrence, the DATA GATE output from formatter logic A3A3 conditions platform logic A3A2 to accept analog-to-digital converter outputs to multiplex the encoded data bits into the 1 KC NRZ DATA output from the address register and digital multiplexer in platform logic A3A2. Upon generation of the CLEAR command from the programmer logic, the last seven stages in the address shift register is set to a ZERO state in order to receive the encoded seven bit digital word. When the SET command from the programmer logic is applied to the data word gates, the seven bit digital word is loaded broadside into the address shift register and shifted into the data bit stream by the 1 KC CLOCK pulses.

3-15. Power Control And Distribution Module A4.

3-16. DC-to-DC Converter and Regulator A4A1.

The dc-to-dc converter and regulator in power control and distribution module A4 are utilized to provide all operating voltages for the circuits within the platform equipment. tt accepts an input voltage of -24.5 vdc and provides this output to transmitter module A1, receiver module A2, and data and ranging module A3. It also supplies ±15 vdc, ±9 vdc, +6 vdc, and +3.4 vdc to data and ranging module A3 in order to drive the logic circuits, analog multiplexer gates, and analog-to-digital converter.

The input -24.5 vdc, from a battery or whatever source is utilized to power the platform equipment, is applied to the regulator which governs the voltage input to the dc-to-dc converter. The regulator is more properly termed a preregulator due to the fact that it regulates the -24.5 vdc input prior to applying it to the dc-to-dc converter. This results in all the output voltages being regulated at the same time instead of one at a time as would be the case if the regulator was positioned on each output line. The dc-to-dc converter utilizes synchronous switching at a 6.25 KC rate and a single transformer whose output windings develop all output voltages. All output voltages from the transformer secondary are rectified and filtered for noise prevention prior to distribution throughout the equipment.

3-17. Relay Control A4A2A3.

The relay control circuits in power control and distribution module A4 are utilized to activate and deactivate latching relays which, in turn, energize and deenergize transmitter module A1 in response to commands from platform logic A3A2 and formatter logic A3A3. The latching relays also provide TELEMETRY HOLDOFF preset voltages to PCM demodulator and bit synchronizer A3A1, platform logic A3A2, and formatter logic A3A3. The pulses that activate and/or deactivate the latching relays are controlled by relay control one shots that are triggered by the proper voltage levels from their respective logic circuits. Proper isolation is maintained by utilization of transformer coupling between the logic circuits and the relay control one shots.

The TRANSMITTER ON command is developed by relay control A4A2 when the address and address correlators in platform logic A3A2 recognize the platform address code

and apply an ADDRESS SYNC pulse to the relay control one-shot. The one shot, in turn, activates a latching relay and applies a +24.5 vdc pulse to transmitter module A1. This pulse prepares the transmitter for transmission of data frame information. At the same time, another set of contacts on this relay open and removes the TELEMETRY HOLDOFF preset voltage from the PCM demodulator and bit synchronizer, platform logic, and formatter logic. Removal of this voltage conditions these circuits to operate in a normal manner. The TRANSMITTER OFF command is developed when the relay control flip-flop receives one of two inputs. One input being the END OF FRAME signal from the framecounters thatsignifies thatnomore analog data is to be encoded and that data frame transmission is complete. The second input being the END OF THREE SECONDS signal from three second counter that indicates some type of malfunction or that the platform did not recognize its address. The TRANSMITTER OFF command is a +24.5 vdc pulse.

3-18. Modulator Driver A4A2A4.

The function of the modulator driver in power control and distribution module A4 is to convert the serial pulse train output from the 12.5 KC modulator in platform logic A3A2 to a suitable signal for modulating the platform transmitter. The modulator driver accepts logic level inputs of the 12.5 KC MODULATED DIGITAL SUBCARRIER and its complement and provides a corresponding signal of the correct level and impedance to the transmitter input. It also provides isolation between logic ground and transmitter ground. The DATA MODULATION output from the modulator driver is ac coupled to the transmitter input to ensure equal deviation in the transmitted output frequency.

3-19. Transmitter Module A1.

The primary power, TRANSMITTER ON/OFF commands, and DATA MODULATION inputs from power control and distribution module A4 are applied to transmitter module A1 through input connector A1J1. The TRANSMITTER ON command occurs upon generation of an ADDRESS SYNC pulse in platform logic A3A2 when the platform address code is recognized. It is a +24.5 volt pulse that allows transmission of the modulated data during satellite interrogation or ISE checkout. The TRANSMITTER OFF command is a +24.5 volt pulse that inhibits data transmission but allows the voltage controlled crystal oscillator (VCXO) and its internal buffer and the power amplifier filaments to remain in operation.

The DATA MODULATION is applied to the VCXO whose operating frequency is 466.00 megacycles. A VCXO output frequency of 58.250 megacycles is provided to the buffer amplifier that provides isolation between the VCXO output and first doubler input with additional power gain. The first doubler provides an output frequency of 116.50 megacycles to the intermediate power amplifier (IPA). The IPA is a solid-state amplifier that increases the first doubler output to a suitable level to drive the varactor frequency doublers and the power amplifier. The 116.500 megacycle input frequency to the varactor second doubler is multiplied to 233.00 megacycles to provide sufficient drive to the varactor third doubler. The varactor third doubler raises the 233.00 megacycle input to 466.00 megacycles in order to drive the power amplifier. The power amplifier is a cavity-tuned grounded-grid amplifier that provides a power output sufficient to apply through the diplexer portion of transmitter module A1. The diplexer in transmitter module A1 is a stable filter that utilizes coaxial

cavities to ensure minimum insertion loss and to allow the utilization of a common antenna by transmitter module A1 and receiver module A2. The input -24.5 vdc operating voltage is converted in the dc-to-dc converter to provide filament voltage and dc plate power for the vacuum tube power amplifier. The dc-to-dc converter also provides telemetry signals for monitoring the power amplifier plate current and the TRANSMITTER ON/OFF commands. The power amplifier temperature, driver module temperature, and transmitter housing temperature are derived and monitored by internally located transducers.

SECTION IV

CHRONOLOGICAL HISTORY

4-0. CHRONOLOGICAL HISTORY.

4-1. GENERAL.

This section of the report provides a discussion of the month-by-month progress and problem areas encountered during this phase of Contract No. NAS5-10278. Work pertaining to this phase of the contract was initiated on 16 August *1966* and continued through May 1967.

4-2. SEPTEMBER *1966.*

The design effort and work performed during this period under Contract No. NAS 5-10278 pertains to the design, development, and testing of three systems of Integration Support Equipment. The design effort during this period progressed satisfactorily with no maior problems. The maior design areas included the self-check tester and the overall equipment rack design. The overall design of the tester was discussed between GSFC and Radiation personnel during the week of *26* September *1966* and agreement was reached as to the amount of quantitative data that would be monitored and displayed. It was agreed that the tester would display a NO GO indication if any monitored parameter was out-of-tolerance but would not indicate the amount and/or type of deviation. It was also agreed that the tester be constructed in such a manner that it could be easily removed from the rackconfiguration for field use. The overall design of the rack configuration, including mounting, interconnections, and layout of the RF components and measuring equipment, was also initiated.

During the first part of the period, all materials necessary to fabricate and assemble the ISE platform units were placed on procurement and was received before the end of the period. The three platform receivers were placed on order through a change order to an existing subcontract with TRW Space Laboratories on Contract NAS 5-9559. The standard test equipment for use in the ISE were also ordered. At this time, no significant problem areas pertaining to long lead time items were expected.

4-3. OCTOBER *1966.*

The preliminary design phase of the Integration Support Equipment (ISE) was completed during this period and all major system concepts were determined. Work completed during the proposal analysis which utilized the TI 51 series integrated circuit modules manufactured by Texas Instruments was discarded in favor of the monolithic DTL 800 series modules manufactured by Radiation incorporated. Also, during this period, the decision was made to incorporate a removable self-check drawer that would be completely operable when powered by the supply used for the Platform Electronics and Telemetry Equipment. Because of this capability, a dc-to-dc converter is required in the self-check drawer. The standard 19-inch removable drawer will be sufficiently assembled to withstand rugged handling during frequent moves without serious damage.

Other design deviations from the proposed configuration of the Integration Support Equipment during this period include a signal routing change and component removal, replacement, and/or addition. The signal routing change resulted in programming the 12.5 KB data output from the ISE through the modblator driver in the platform power control and

distribution module. This method of signal routing implemented verification of existing circuits and a significant reduction in the number of components. The addition of a red NO GO indicator lamp allows the operator to observe the changing status of the functional circuits within the ISE. The deletion of a variable RF attenuator from the self-check loop is a resultant of judicious selection of fixed attenuators and coaxial switching in the RF control drawer and self-check drawer.

Another design change accomplished during this period was the replacement of the PNP 2N2907A transistors in the proposed dc-to-dc converter with the less expensive 2N3741 type of component. This change represented a cost savings while an increased upper temperature limit was realized through a greater thermal dissipation of the transistor. A problem area encountered during this time involved the 64.5 megacycle local oscillator in the self-check drawer. Greenray Industries was selected as the original vendor but was eliminated in favor of Accutronics Incorporated due to delivery schedule slippage of their first unit.

4-4. NOVEMBER 1966

Several electrical and mechanical changes were incorporated during this period that deviated from the proposed approach. The arrangement for the rack-installed equipment was modified for ease of testing and handling while electrical modifications to the RF control drawer and self-check drawer were incorporated to increase the operational capabilities and parameters of the equipment.

Modifications to the RF control drawer included a rearrangement of the attenuation and operating mode switches on the front panel and the addition of a fixed 80 db of attenuation that prevents application of unattenuated transmitter output power to the self-check mixer. In addition, the mixer, 64.5 megacycle oscillator, RF converter, and 80 and 15 db attenuators were relocated to the self-check drawer in order to utilize the tester to check platforms external to the rack.

Modifications to the self-check drawer included relocating the functional circuits between the platform data and ranging module and power control and distribution module. This modification eliminated the necessity of an additional modulator and also reduced the logic circuits required. The logic circuits were also functionally simplified by inverting the generated address range pattern instead of requiring address and address complement verification circuits. Also, the functional operation of the logic circuits was further simplified by the addition of a unique data verifier that recognizes the four-bit difference between the data word codes for the zero-scale, half-scale, and full-scale simulated transducer inputs. The logic was also modified to check platforms with six hardwired input data channels.

The mechanical and electrical design of the equipment was completed and all purchased assemblies, except the power meter and S-meter for system 1 and the event recorder for systems 2 and 3, were received during this period. Progress pertaining to assembling the various ISE mechanical structures in a final configuration during this period appeared to be at a virtual standstill. First of all, the equipment rack housings received from the vendor were damaged during shipment and needed immediate repairs prior to incorporating the mounting hardware. Due to scheduling and funding problems, the maintenance department

at Radiation Incorporated repaired the racks. The mechanical assembly of all units progressed as rapidly as the mounting hardware was received from the machine shop.

Another delay encountered during this period again involved the vendor-supplied 64.5 megacycle oscillator in the self-check drawer, During initial testing and fabrication of the oscillator, Accutronics Incorporated determined that due to the required rigidness and shielding, the design of the enclosure had to be modified. This design change necessitated a layout change in the completed assembly drawing of the self-check drawer which thus, delayed fabrication of the units. In addition, the electronic technicians fabricated a dummy self-check drawer and dummy panels in order to implement initial checkout of the self-check drawer. Initial checkout of the self-check drawer was delayed an additional week by transferring a single-ended wire list to a double-ended list of the drawer.

The wiring on all logic printed-circuit cards in the self-check drawer for system 1 was completed and all integrated-circuit modules were mounted on the cards. The internal drawer wiring, using a dummy front panel, was 95 percent completed. Wiring on the AC distribution panel was completed and tested and the fabrication of the analog and RF control panels was initiated. Also, the fabrication of the power supply card for system 1 was 75 percent completed.

During this period, fabrication and assembly of the ISE platforms was delayed until the last of the period by delivery of the MOS-FET gates. Delivery of these gates during this period was accomplished due to relaxation of the leakage current specification. Regardless of the delay, the assembly of the platform for ISE system 1 was approximately 25 percent completed with 80 percent of the cordwood submodules completed and card installation of integrated circuits initiated. Module construction for the platforms to be utilized in systems 2 and 3 was also initiated.

4-5. DECEMBER 1966.

Final fabrication and assembly of the first ISE rack were initiated during this period and two rack configuration modifications were incorporated into the final product. The overall equipment rack was designed to use foot-lock devices to stabilize the equipment after positioning in its operating area. The method of rack stabilization was changed due to resiliency of the foot-lock spring causing an unsteady condition after emplacement. This condition was absolved by utilization of caster wheels with locking devices which ensures that all four wheels contorm to the surface contour and provides firm support at the four corners. Another configuration change ot a mechanical nature involved relocation ot the AC distribution panel from its original position directly behind the blower assembly to an area directly behind the power meter and voltmeter panel. This modification was necessary because the AC distribution panel was not allowing the forced air from the blower to througkly circulate over the enclosed equipment. The power supply printed-circuit card (A1) in the self-check drawer was also repositioned because of insufficient space due to the size ot the input power transformer.

Minor circuit modifications to the self-check drawer were also accomplished during this period. One modification added an overvoltage protection circuit to the self-check

drawer that prevents damage to the internal circuits or platform modules if the power supply becomes unregulated. The second modification included the addition of an extra power filter network on the power supply printed-circuit card. This modification improved the efficiency of the circuit and provided power isolation for the remaining cards by reducing the load through the input inductor which, in turn, reduces a voltage drop due to the resistance of the inductor to allow a higher voltage output from the preregulator.

During electrical checkout of the vendor-supplied 25 KC oscillator used for system timing pulse generation, it was discovered that the accuracy of the unit was not within specification. The unit was returned to the vendor for adjustment and calibration.

Also, during this period, the vendor supplied power meters and S-meters were received while the event recorders for systems 2 and 3 were still on order.

4-6. JANUARY 1967.

During this period, the government furnished IRLS time delay simulators received during the previous period were examined for damage and operational malfunctions. It was necessary to modify and repair a broken phenolic printed-circuit board prior to actual electrical checkout. The simulator was checked using an IRLS Satellite to verify the actual delays according to the tront-panel switch positions. The 0 microsecond delay position of the switch on all units was inaccurate as much as five microseconds. The inaccuracy ot this switch position was remedied by rewiring the switch to provide the correct delay indication. It was decided that no other switch positions would be rewired or moditied and that a time delay calibration chart would be provided with the individual systems. Numerous bad solder joints were also detected and repaired during the electrical checkout process.

The electrical check of the self-check drawer design was also initiated during this period. Completion of the check was delayed due to problem areas involving the IRLS Satellite power control and distribution module. These problem areas pertained to a short circuit between an internal printed-circuit card and cordwood submodule located on the card and necessitated modification of all power control and distribution modules in the IRL Subsystem. A complete detailed report of the problem areas and corrective action is provided in GSFC Malfunction Reports 11253 and 11254 and the IRLS Final Report dated June 1967, Fabrication, assembly, and testing of the ISE data and ranging modules also delayed self-check testing.

Utilization ot a ditferent platform configuration and a dummy self-check drawer fabricated by engineering technicians enabled initial checkout of the drawer. During the checkout process, the NASA Technical Officer discovered that the self-check data translator circuits did not detect and verify the presence of an unique N-word or all eight minor bits of the M-word. This verification process was desired and an engineering sketch of the functional logic circuits required was torwarded to the technical officer for inspection and approval. Laboratory evaluation and test of the proposed modification to the data translator circuits determined that the 12.5 KC clock output generated by the T151 series integrated circuits and the Radiation 800 series integrated circuits were not compatible. This incompatibility necessitated an additional modification to the translator circuits. The additional

modification did not use internally generated timing signals from the platform modules to accomplish its assigned tasks but operated by using the plattorm data output only. Incorporation of the various modifications satisfied the technical officer's requirements that the data translator recognize and verity the eight minor bits of a M-word representing a logic ONE and that an unique N-word occurs during the last four minor bits of the tirst 1 KC bit of a 16-bit stream. This particular modification also necessitated the addition of another shift-register stage in the address and data correlator shift register.

The event recorders for systems 2 and 3 were also received during this period and rack equipment integration was completed except for the RF control and selt-check drawers.

4-7. FEBRUARY 1967.

Two major problem areas were encountered during this period. One area involved the 64.5 megacycle local oscillator in the selt-check drawer that is manufactured by Accurtronics Incorporated. During functional checks of the equipment, it was discovered that the oscillator generated a large seventh harmonic frequency and second harmonic frequencies from two through six. Generation of the seventh harmonic of 451.5 megacycles caused the input to the receiver in the RF control drawer to oscillate. The local oscillator in the platfotm receiver generates a frequency of 426.5 megacycles, therefore, the seventh harmonic from the self-check oscillator is the image frequency of 401.5 megacycles. The 64.5 megacycle oscillators were returned to Accutronics Incorporated for rework. Rework of the units consisted of adding a filter circuit and changing the attenuation configuration (from input of mixer to output of mixer) such that the ratio between the desired carrier and seventh harmonic will be significantly larger (60 dbm) than any harmonic frequency passing through the self-check mixer.

The second major problem encountered during this period resulted from connecting all ground points on the self-check printed-circuit cards in series. This method of ground interconnection created ground loops and a difference in ground potential between the various card grounds. This problem was remedied by connecting all printed-circuit card grounds to a central point.

4-8. MARCH 1967.

Part of the hardware portion of the Integration Support Equipment was completedduring this period by acceptance testing system 1. Several problem areas hampered the completion of the system 1 testing program but were satisfactorily resolved in time to accomplish the schedule. These problem areas involved individual component and module malfunctioning and equipment operating parameters. The problem area encountered during checkout of system 1 pertained to the frame error flip-flop in the self-check error recognizer beingtriggered by the steering inputs. This problem was resolved by application of supply voltages to the steering inputs and gating the clock pulse inputs. Checkout of system 2 uncovered a problem area pertaining to the address and data recognition processes in fhe data translator. With no carrier frequency present, the video output from the platform receiver is random noise which is capable ot being decoded into a random data pattern. In turn, the platform is capable of encoding a random pattern which, in the self-check mode, is monitored by the data translator.

Since the data translator monitors the data at all times, it therefore, will decode the correct address at random intervals. Recognition of the correct address code after the platform is apparently denergized, causes a false count in the error recognizer and thus, an erroneous NO GO condition. Solution of this condition was implemented by inhibiting the data translator circuits by the error threshold signal level from the platform. During checkout of ISE system 3, a regulated transistor in the event recorder was burned up but was immediately repaired by a service engineer from the Hewlett Packard Company. Another problem area pertaining to system 3, involved the platform transmitter which was returned to TRW Space Technology Laboratories due to an erroneous center frequency at low voltage. Both system 2 and system 3 were scheduled to complete acceptance testing during the April reporting period.

4-9. APRIL **1967.**

System 1 of the Integration Support Equipment was delivered to General Electric, Valley Forge, Pennsylvania during this reporting period. Due to the overall height of the equipment rack, the unit could not be installed into the Nimbus equipment vehicle. Because of the rack incompatibility, the rack-mounted equipment will be transferred to a shorter rack with the storage drawer and blank panel deleted. Equipment transfer will be accomplished at the Nimbus integration facility when it will not conflict with spacecraft integration and testing.

Acceptance testing of systems 2 and 3 was also completed during this period with both units being retained at Radiation incorporated for shipping instructions. As mentioned in the previous reporting period, the transmitter for system 3 was unable to meet thecenter frequency tolerance specification of the temperature range and returned to the vendor for adjustment. The center frequency/temperature deviation could not be corrected and the unit was returned to Radiation Incorporated. The unit was accepted and reinstalled in system 3, because large variations in ambient temperature are not anticipated during system operation.

4-10. MAY **1967.**

System 2 of the Integration Support Equipment was delivered to the NASA/GSFC, Greenbelt, Maryland during this reporting period and system 3 was retained at Radiation Incorporated. System 3 will be utilized for checkout and test of five GO/NO GO test sets required under Modification Number Two of this contract.

SECTION V

CONCLUSIONS AND RECOMMENDATIONS

5-0. CONCLUSIONS AND RECOMMENDATIONS.

5-1. CONCLUSIONS.

The results from testing performed at Radiation Incorporated located in Melbourne, Florida and the General Electric facility at King of Prussia, Pennsylvania indicate a high degree of confidence that the Integration Support Equipment will perform its specified mission during the Nimbus B flight. The designated mission of the ISE includes preflight checkout of the IRLS satellite during integration with the Nimbus spacecraft or immediately prior to launch, normal satellite-to-platform operation, self-check operation, and fieid-checkout of standard JRLS platform,

5-2. RECOMMENDATIONS.

Based upon experience gained during completion of the ISE phase of Contract No. NAS5-10278, Radiation Incorporated recommends packaging and equipment versatility changes be included in future IRLS experiments and operational systems. Each category of changes is discussed in the following paragraphs.

5-3. Versatility.

The self-check drawer used in the IRLS Integration Support Equipment was designed and constructed in such a manner that it may be removed from the rack configuration for field checkout of a standard IRLS platform. It would be practical to fabricate a self-check tester for each platform currently in use. It is also recommended that the logic circuits that generate a GO or NO GO indication be redesigned and modified to indicate a trouble or malfunctioning area. The practicality of this modification would be greatly enhanced by a repackaging effort.

5-4. Packaging.

The final packaging design of the self-check drawer resulted from a trade-off of the two basic requirements of being rack-mounted and field transportable. By utilizing experience gained during the completion of this phase, Radiation incorporated recommends that the unit can be significantly reduced in size and weight by reevaluating the packaging concept. Shielding of the integrated circuit modules and a rerouting of the integral cable assemblies could also be accomplished by repackaging.

APPENDIX I

GSFC SPECIFICATION
IRLS INTEGRATION
SUPPORT EQUIPMENT

S-731-P-20
January 7, 1966

GSFC SPECIFICATION

IRLS INTEGRATION

SUPPORT EQUIPMENT

GODDARD SPACE FLIGHT CENTER

GREENBELT, MARYLAND

INTEGRATION SUPPORT EQUIPMENT

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4. NOTES

1. SCOPE

This specification defines the requirements for the IRLS integration Support Equipment (ISE). The scope of the work shall include the design, fabrication, and testing of a self-contained rack mounted test set which provides the necessary functional tests to confirm proper operation of the IRLS.

2. REQUIREMENTS

The ISE shall consist of an IRLS platform, power supplies, and auxiliary test equipment which will provide the necessary information to confirm proper spacecraft subsystem operation of the IRLS during pre-launch and post launch operations. A block diagram of the system is shown in Figure 1.

2.2 CONFIGURATION

2.2.1 Size

The equipment shall be mounted in a standard size ventilating rack. All input/output interfaces and controls shall be clearly identified.

2.2.2 Design Standard

All electrical designs shall be identical to those existing for IRLS platforms under NASA/IRLS Contract NAS5-9559. This includes design components as well as configurations, but does not necessarily apply to packaging.

2.3 PLATFORM ELECTRONICS

The platform electronics shall consist of a radio communication system and a PCM decoding and signal conditioning system. The design specifications concerning RF frequencies, bit rates, ranging pattern, etc., shall conform to the requirements for IRLS platforms as per NASA-IRLS Specification (including latest modifications) dated February 1964. The circuit designs shall conform to the requirements of paragraph 2.2.2 above.

2.4 PLATFORM CONTROLS

2.4.1 Analog Channel Inputs

The analog channel input signals shall consist of either manually adjustable precision voltage levels, provided by an internal power supply, or external voltages derived from sensors or other sources. For the latter case, the channel inputs shall be conveniently accessible.

2.4.2 Address Selection

The capability for manually programming 16 bit platform addresses shall be provided. The output impedance and voltage characteristics (seen by the platform logic) of each bit shall be identical to the hard wire characteristics of regular platform addresses.

2.4.3 Frame Selection

The number of transmitted frames shall be manually selectable from a panel control switch (one to six per interrogation).

2.4.4 Transmitter Signal Level

The transmitter output power level shall be adjustable from zero to 120 db through the insertion of RF attenuators. Sufficient attenuators, directional couplers, and an RF power meter shall be provided and conveniently located.

2.4.5 Time Delay Simulator

A time delay simulator providing delays from zero to 2000 micro-sec. shall be supplied by NASA. The contractor shall integrate the simulator into the ISE between the transmitter modulator driver and the transmitter modulator input as shown in Figure 2. The simulator specifications are shown in the notes.

2.5 TEST AND RECORDING REQUIREMENTS

2.5.1 Self Tester

Internal testing functions shall provide but not be limited to, the following capabilities:

1. Address Verification
2. Correctly encode and format one or more data frames
3. Measurement of RF power
4. Measure all power supply voltages
5. Measure all clock frequencies

2.5.2 Indicating Lamps

Indicating lamp displays may be used, wherever feasible, to indicate the occurrence of significant events and/or to display time codes, addresses, etc.

2.5.3 Timing information

The time of occurrence of significant events shall be permanently recorded, on a chart recorder, during each interrogation. This shall include initial time intercept, receipt of address complement, acquisition of phase lock, and the total satellite transmitting time.

2.5.4 Receiver Signal Power

The platform 25 mc RF signal shall be detected, indicated, and measured upon receipt of the satellite transmission.

2.6 POWER SUPPLY

A power supply operating from 117 volts AC shall be included in the equipment. The supply shall provide DC voltages to the platform connector and to auxiliary equipment as necessary.

2.7. REPORTS

2.7.1 Progress Reports

The contractor shall submit to the Technical Officer monthly progress reports and a final project report in accordance with GSFC-TID-S-100.

2.7.2 Instruction Manual

The contractor shall provide one (1) reproducible and six (6) copies of an instruction manual to be delivered concurrently with each ISE. The contents of the manual shall include, but not necessarily be limited to:

1. Discussion of circuits
2. Operation procedures
3. Block diagrams
4. Schematic diagrams
5. Electrical interfaces
6. Timing diagrams
7. Parts list
8. Design specifications

2.8 DRAWINGS

The contractor shall provide one reproducible and one copy set of the latest drawings, schematics, parts lists, etc., to the Technical Officer upon request.

3. PREPARATION FOR DELIVERY

The contractor shall provide any packaging and shipping containers required for the safe transport of the systems to designated points.

4. NOTES

Time Delay Simulator Specifications

1. Power Supply

Voltage	110-120 VAC, 60 cps

2. Delay

Switch Positions	12
Resolution	80 microseconds
Accuracy	0.5 ±.1 microsecond
Maximum Delay	2000 microseconds
Minimum Delay	Zero (0)

3. Clock Input

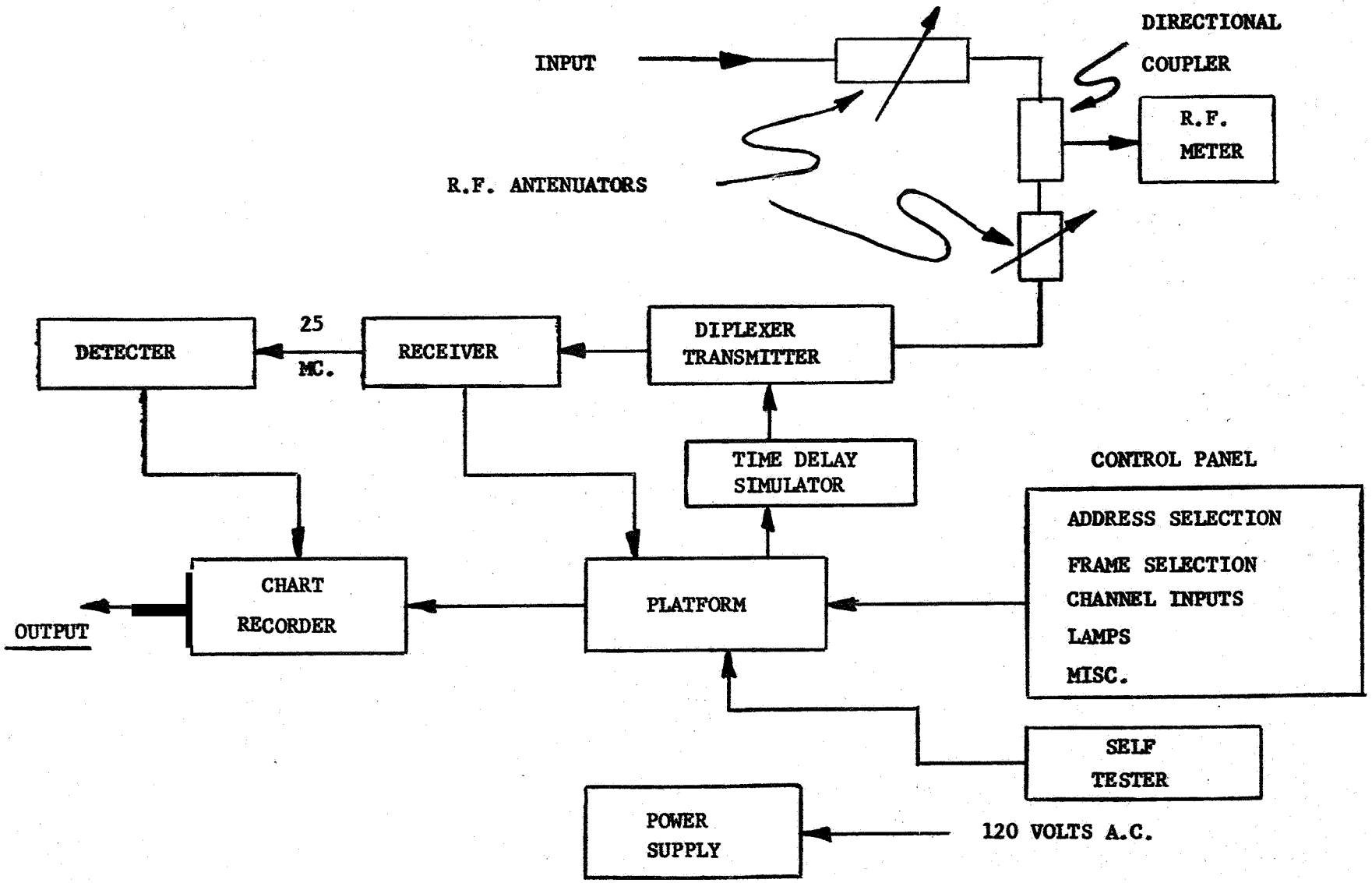
Frequency	12.5 kc
Level	2.5 V. P-P
Input Impedance	3 Kohms

4. Signal Input

Characteristic	NRZ
Frequency	12.5 KB/sec.
Amplitude	± 2.5 V. P-P
Input Impedance	20 Kohms

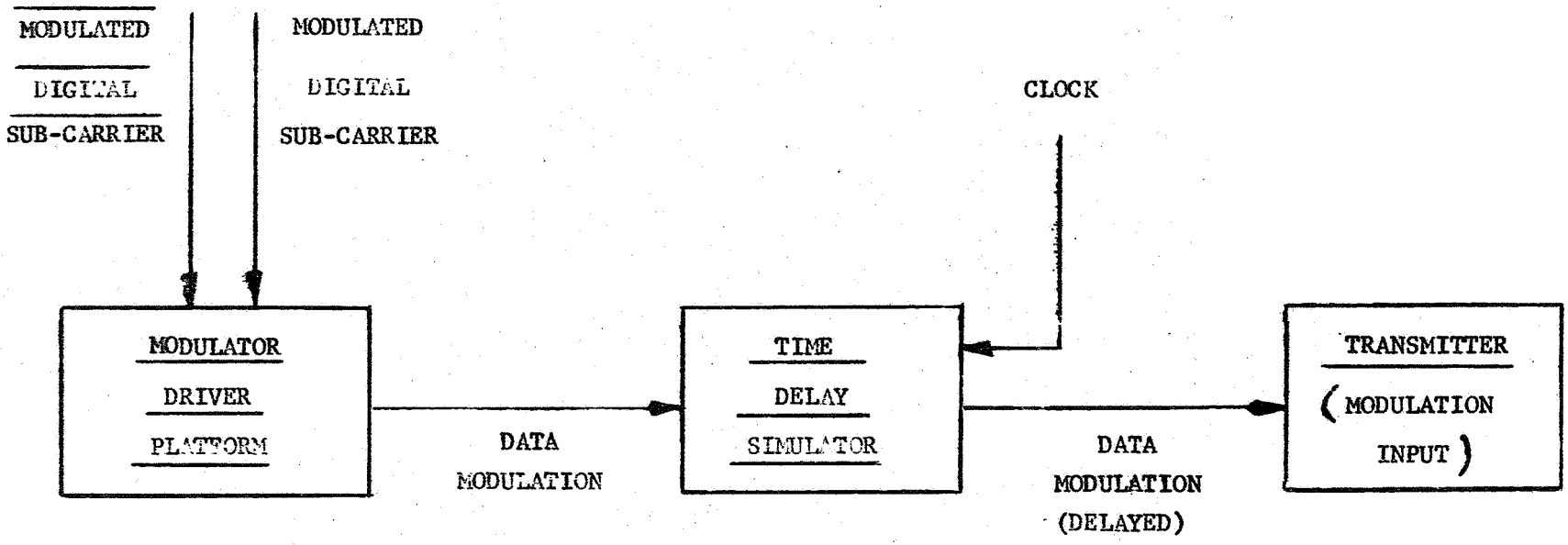
5. Signal Output

Characteristic	NRZ
Frequency	12.5 KB/sec.
Source Impedance	100 ohms



BLOCK DIAGRAM

FIGURE-1



TIME DELAY SIMULATOR
INTEGRATION

FIGURE-2